HOLTEK

HT32F65232
Datasheet

32-Bit Arm® Cortex®-M0+ BLDC Microcontroller,
up to 32 KB Flash and 4 KB SRAM with 2 MSPS ADC,
CMP, OPA, USART, UART, SPI, I^2C, MCTM, GPTM,
SCTM, BFTM, CRC, LSTM, WDT, DIV and PDMA

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1 General Description

The Holtek HT32F65232 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The device operates at a frequency of up to 60 MHz with a Flash accelerator to obtain maximum efficiency. It provides 32 KB of embedded Flash memory for code/data storage and 4 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as Hardware Divider DIV, ADC, OPA, CMP, I^2C, USART, UART, SPI, MCTM, GPTM, SCTM, BFTM, CRC-16/32, LSTM, WDT, PDMA, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as electric scooters, kitchen ventilators, vacuum cleaners, pumps, funs and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 60 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 32 KB on-chip Flash memory for instruction/data and options storage
- 4 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F65232 device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator to obtain maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-Out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by external signals, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control Unit, CKCU, provides a range of oscillator and clock functions. These include High Speed Internal RC oscillator (HSI), High Speed External crystal oscillator (HSE), Low Speed Internal RC oscillator (LSI), Phase Lock Loop (PLL), HSE clock monitor, clock prescaler, clock multiplexer, APB clock divider and gating circuitry. The clocks of AHB, APB and Cortex®-M0+ are derived from system clock (CK_SYS) which can come from HSI, HSE, LSI or system PLL. Watchdog Timer (WDT) and Low Speed Timer (LSTM) use the LSI as their clock source.

Power Management Control Unit – PWRCU

- Single V_{DD} power supply: 2.5 V to 5.5 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- Two power domains: V_{DD} and V_{CORE} power domains
- Two power saving modes: Sleep and Deep-Sleep modes

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides two types of power saving modes which are the Sleep and Deep-Sleep modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate wake-up events or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 2 Msps conversion rate
- Up to 12 external analog input channels

A 12-bit multi-channel Analog to Digital Converter is integrated in the device. There are multiplexed channels, which include 12 external channels on which the external analog signal can be supplied and 3 internal channels. If the input voltage is required to remain within a specific threshold window, the ADC analog watchdog function will monitor and detect the signal. An interrupt will then be generated to inform the device that the input voltage is higher or lower than the set thresholds. There are three conversion modes to convert an analog signal to digital data. The A/D conversion can be operated in one shot, continuous and discontinuous conversion modes.

Operational Amplifier – OPA

- Fixed dedicated I/O pins
- Internal output paths to the A/D converter or comparator
- Input offset calibration
- 10-bit DAC offset voltage

Comparator – CMP

- Two rail-to-rail comparators
- Each comparator has configurable inverting or non-inverting inputs used for flexible voltage selection
  - Dedicated I/O pins
  - Internal voltage reference provided by 8-bit scaler – CMP0 only
  - Internal operational amplifier output
- Programmable hysteresis
- Programming response speed and power consumption
- Comparator output can be routed to I/O pin or to multiple timers or ADC trigger input

- 8-bit scaler can be configured to dedicated I/O for voltage reference
- Configurable inverting input from CMP0N, CMP1N or CVREF
- Interrupt generation capability with wakeup from Sleep or Deep Sleep mode through the EXTI controller

Two general purpose comparators are implemented within the device. They can be configured either as standalone comparators or combined with different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or waking up the MCU from the Sleep or Deep Sleep mode through the EXTI wakeup event management unit.

I/O Ports – GPIO

- Up to 44 GPIOs
- Port A, B, C are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 44 General Purpose I/O pins, GPIO, named PA0 ~ PA15, PB0 ~ PB15 and PC0 ~ PC11 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge-aligned and center-aligned counting modes
- Single Pulse Mode Output
- Complementary outputs with programmable dead-time insertion
- Break input signals to assert the timer output signals in reset state or in a known fixed state

The Motor Control Timer, MCTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), one 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes which include input signal pulse width measurement, output waveform generation for signals such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and break input.

General-Purpose Timer – GPTM

- 16-bit up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge-aligned and center-aligned counting modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder and Pulse/Direction Mode
- Master/Slave mode controller

The General-Purpose Timer, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM outputs. The GPTM also supports an encoder interface using a quadrature decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge-aligned counting mode

The Single Channel Timer, SCTM, consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare match up-counter – no I/O control features
- One shot mode – stops counting when compare match occurs
- Repetitive mode – restarts counter when compare match occurs

The Basic Function Timer, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shot pulses or generate repetitive interrupts. The BFTM can operate in two modes which are repetitive and one shot modes. In the repetitive mode, the counter is restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuitry that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Low Speed Timer – LSTM

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and wake-up control

The Low Speed Timer, LSTM, circuitry includes the APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. The LSTM circuits are located in the V_{CORE} power domain. When the device enters the power-saving mode, the LSTM counter is used as a wakeup timer to let the system resume from the power saving mode.

Inter-Integrated Circuit – I^2C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I^2C module is an internal circuit allowing communication with an external I^2C interface which is an industry standard two-wire serial interface used for connection to external hardware. These two serial lines are known as a serial data line SDA, and a serial clock line SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode; 400 kHz in the Fast mode; 1 MHz in the Fast plus mode. The SCL period generation registers are used to set different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I^2C module also has an arbitration detection and clock synchronization function to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface– SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to (f_{PCLK}/16) MHz for asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer

- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes an 8-level transmitter FIFO, (TX_FIFO) and an 8-level receiver FIFO (RX_FIFO). The software can detect a USART error status by reading USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm and is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger sources:
  ADC, SPI, USART, UART, I^2C, MCTM, GPTM, SCTM and software request

The Peripheral Direct Memory Access circuitry, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed/unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and requires a software triggered start signal by controlling the “START” bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 48-pin LQFP, 32-pin QFN and 24-pin SSOP packages
- Operation temperature range: -40 °C to 105 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F65232
Main Flash (KB)		31
Option Bytes Flash (KB)		1
SRAM (KB)		4
Timers	MCTM	1
	GPTM	1
	SCTM	4
	BFTM	2
	WDT	1
	LSTM	1
Communication	USART	1
	UART	1
	SPI	1
	I^2C	1
PDMA		6 channels
Hardware Divider		1
CRC-16/32		1
EXTI		16
12-bit ADC Number of channels		1 12 channels
Comparator		2
Operational Amplifier		1
GPIO		Up to 44
CPU frequency		Up to 60 MHz
Operating voltage		2.5 V ~ 5.5 V
Operating temperature		-40 °C ~ 105 °C
Package		48-pin LQFP, 32-pin QFN and 24-pin SSOP

Block Diagram

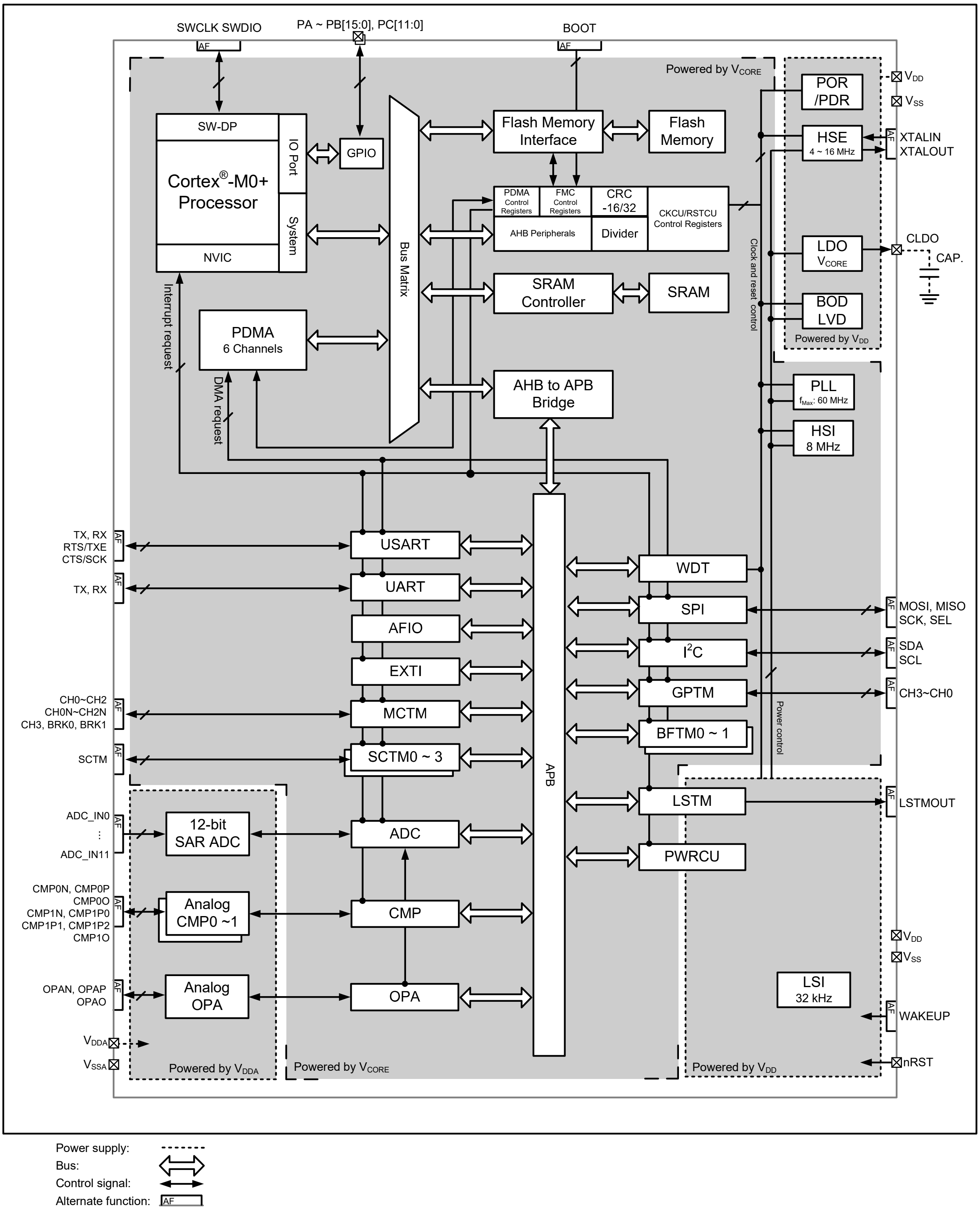


Figure 1. Block Diagram

Memory Map

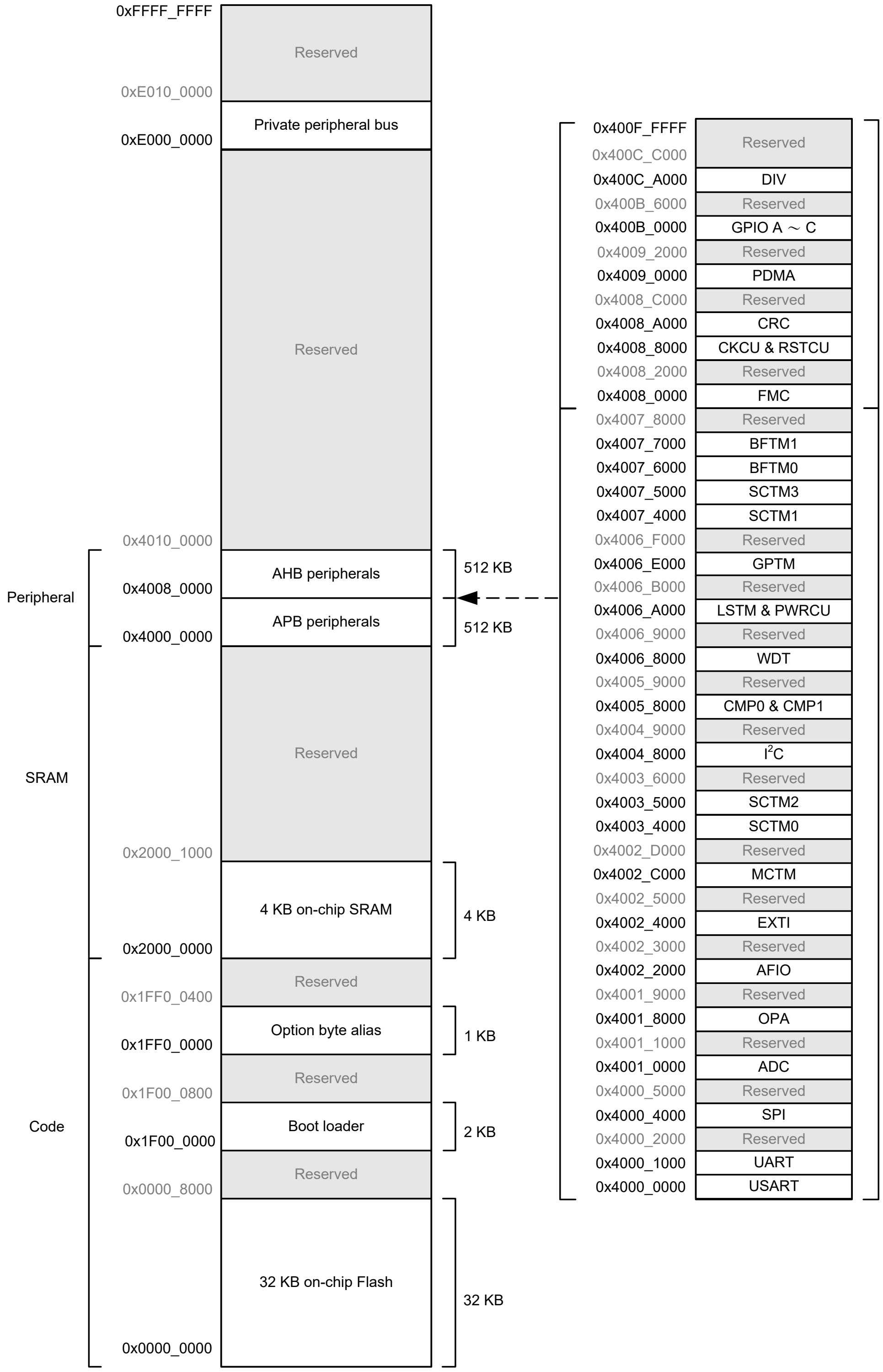


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4001_7FFF	Reserved	
0x4001_8000	0x4001_8FFF	OPA	
0x4001_9000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4005_7FFF	Reserved	
0x4005_8000	0x4005_8FFF	CMP0 & CMP1	
0x4005_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	LSTM & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

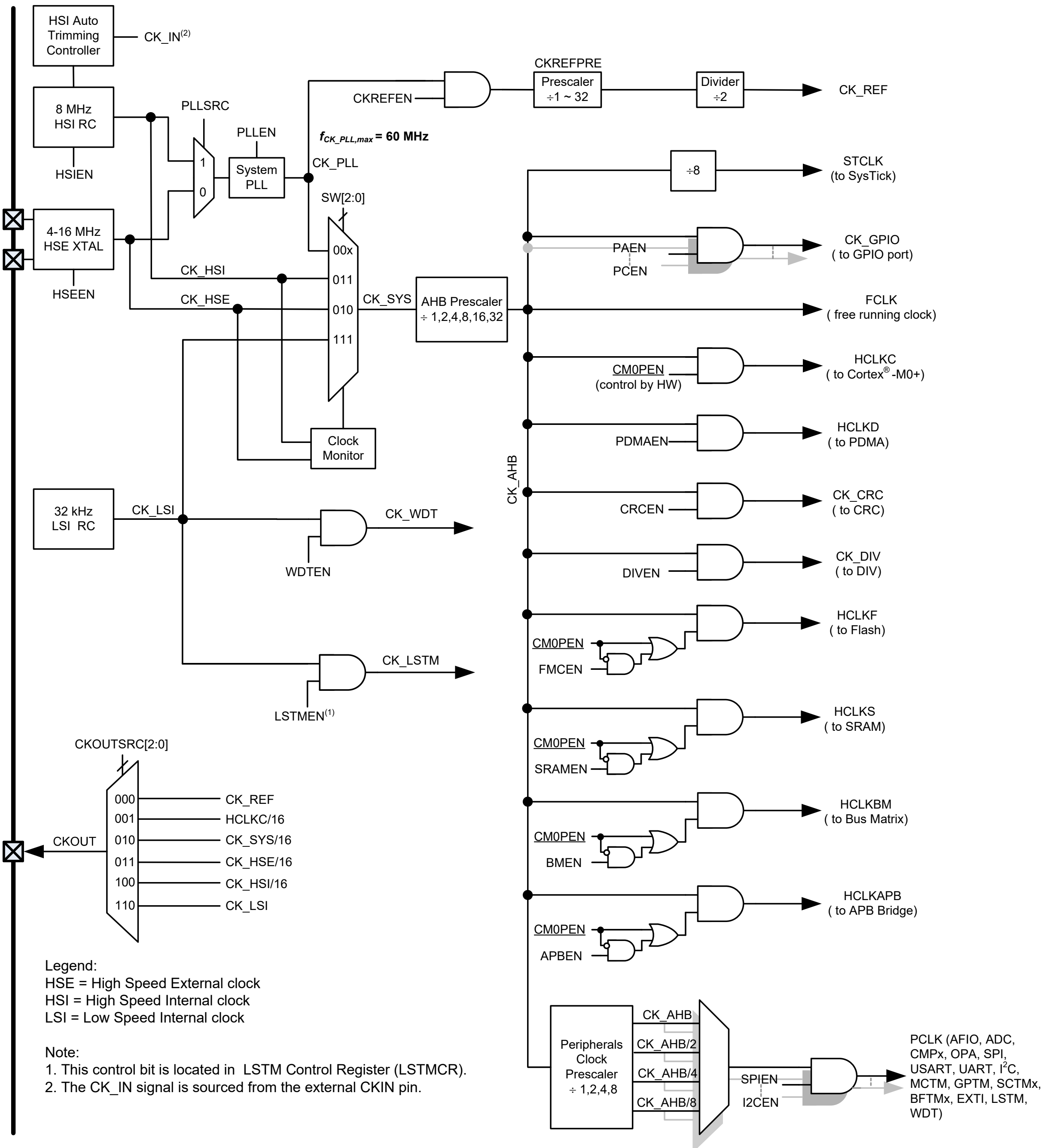


Figure 3. Clock Structure

4 Pin Assignment

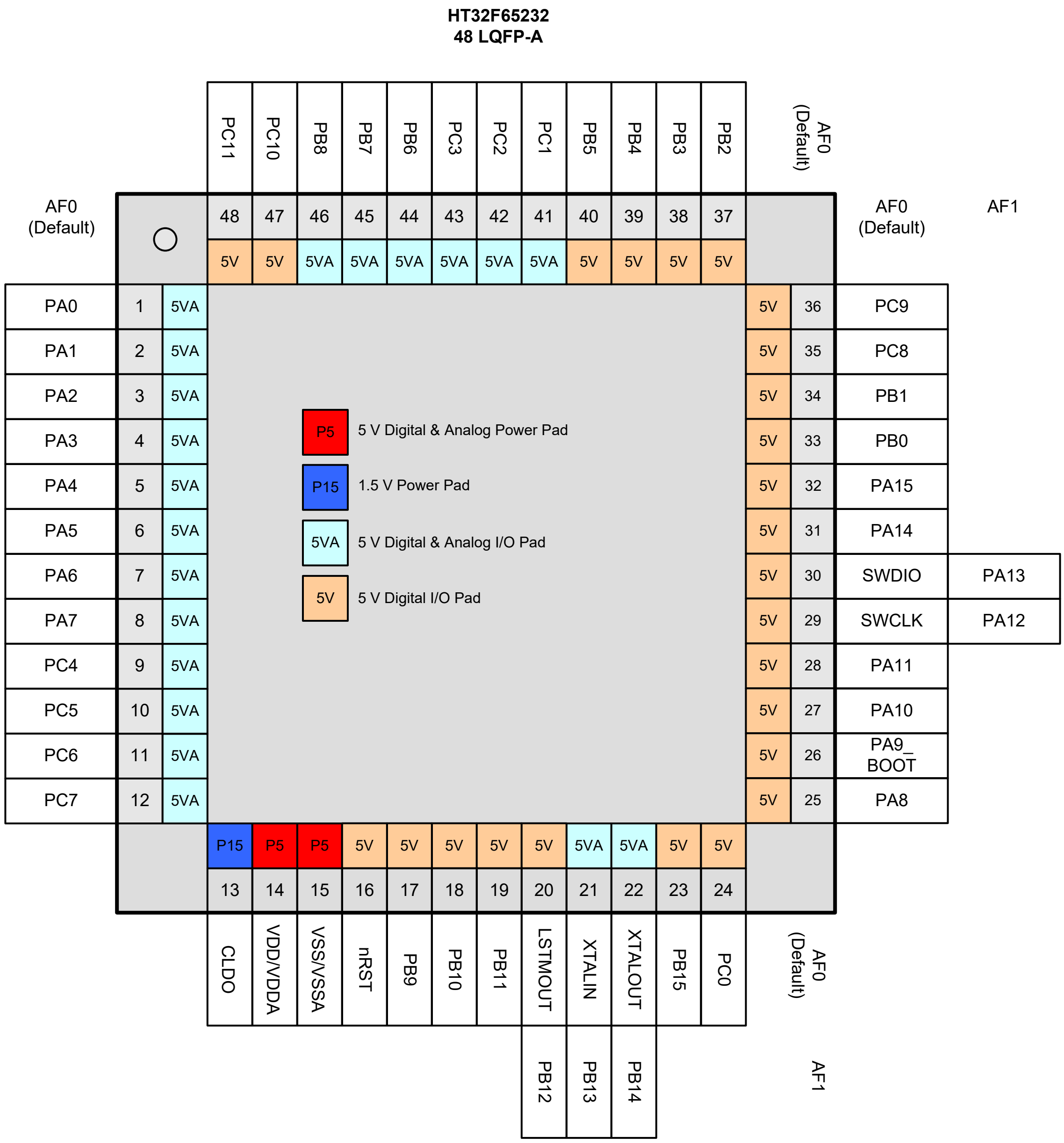


Figure 4. 48-pin LQFP Pin Assignment

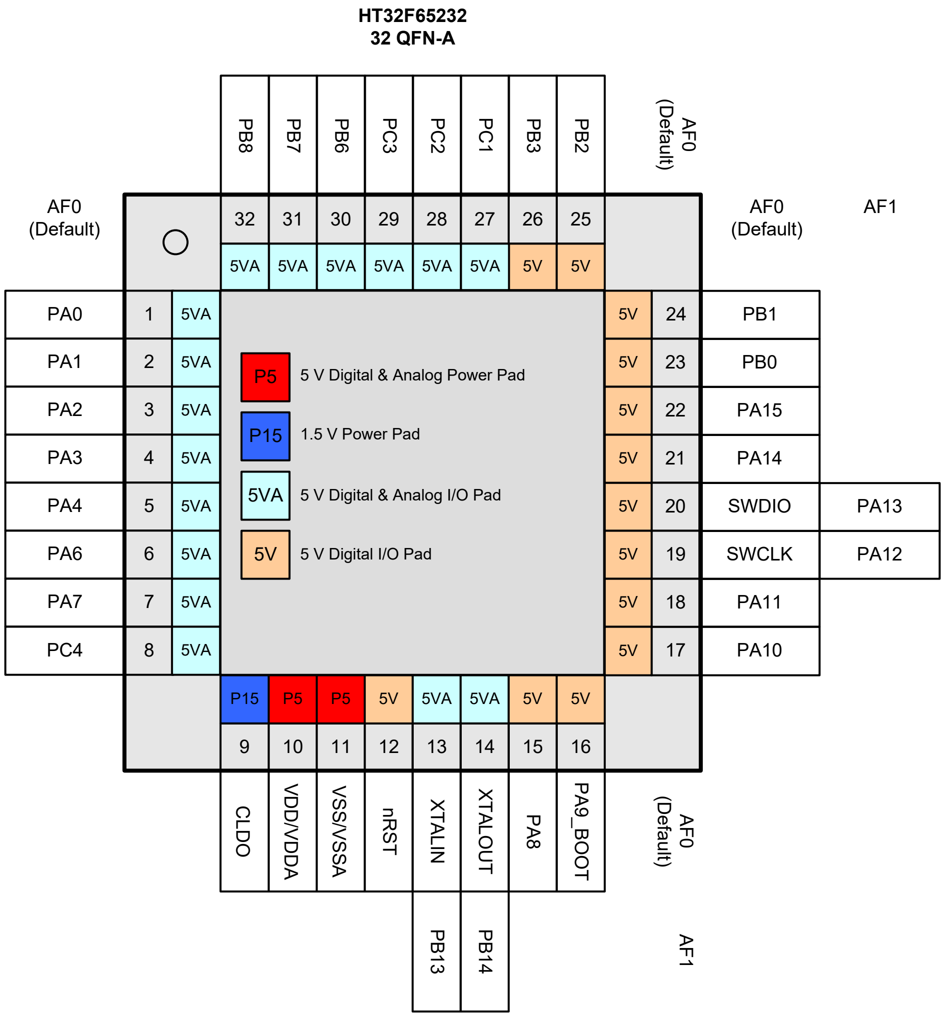


Figure 5. 32-pin QFN Pin Assignment

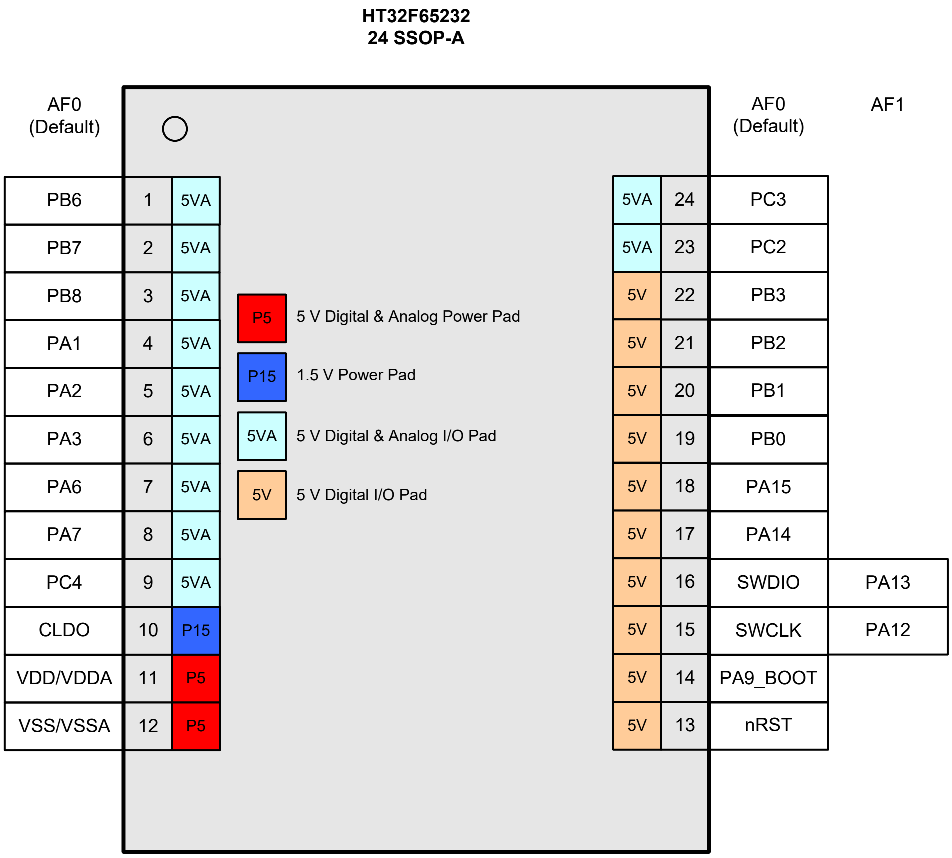


Figure 6. 24-pin SSOP Pin Assignment

Table 3. Pin Alternate Function

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
48 LQFP	32 QFN	24 SSOP	System Default	GPIO	ADC	N/A	GPTM/ MCTM	SPI	USART/ UART	I^2C	CMP/ OPA	SCTM	N/A	N/A	N/A	MCTM	MCTM	MCTM/ System Other
1	1		PA0		ADC_IN5				USR_RTS			SCTM0						
2	2	4	PA1		ADC_IN6				USR_RX	I2C_SCL		SCTM1						
3	3	5	PA2		ADC_IN7		MT_BRK0	SPI_SCK	USR_CTS		CMP0O							
4	4	6	PA3		ADC_IN8		MT_BRK1	SPI_MISO	USR_TX	I2C_SDA	CMP0N							
5	5		PA4					SPI_SEL	UR_TX	I2C_SCL	CMP0P	SCTM2						
6			PA5					SPI_MOSI	UR_RX	I2C_SDA		SCTM3						
7	6	7	PA6								OPAP							
8	7	8	PA7				GT_CH0				OPAN	SCTM2						
9	8	9	PC4				GT_CH1	SPI_MOSI	USR_TX		OPAO							
10			PC5		ADC_IN9		GT_CH2	SPI_MISO	USR_RX			SCTM0						
11			PC6		ADC_IN10		GT_CH3	SPI_SEL	USR_RTS									
12			PC7		ADC_IN11			SPI_SCK	USR_CTS			SCTM3						
13	9	10	CLDO															
14	10	11	VDD/VDDA															
15	11	12	VSS/VSSA															
16	12	13	nRST															
17			PB9						USR_RX			SCTM1						
18			PB10						UR_RX	I2C_SCL								
19			PB11						UR_TX	I2C_SDA								
20			LSTMOUT	PB12					USR_TX			SCTM0						WAKEUP
21	13		XTALIN	PB13			MT_CH3		USR_RTS									
22	14		XTALOUT	PB14			MT_BRK0	SPI_SCK	USR_CTS			SCTM1						
23			PB15					SPI_MOSI				SCTM2						
24			PC0					SPI_MISO				SCTM3						
25	15		PA8				GT_CH0	SPI_SCK	USR_TX	I2C_SCL		SCTM0						
26	16	14	PA9_BOOT				GT_CH3	SPI_SEL	USR_RX	I2C_SDA								CKOUT
27	17		PA10				GT_CH1	SPI_MISO				SCTM3				MT_CH2N	MT_CH2	
28	18		PA11				GT_CH2	SPI_MOSI								MT_CH2	MT_CH2N	MT_CH1
29	19	15	SWCLK	PA12					UR_RX	I2C_SCL								
30	20	16	SWDIO	PA13					UR_TX	I2C_SDA								
31	21	17	PA14				MT_CH2N									MT_CH2		MT_CH2N
32	22	18	PA15				MT_CH2					SCTM2				MT_CH2N	MT_CH1	MT_CH1N
33	23	19	PB0				MT_CH1N									MT_CH1	MT_CH0	MT_CH0N
34	24	20	PB1				MT_CH1					SCTM1				MT_CH1N	MT_CH2	MT_CH2N
35			PC8				MT_CH0N									MT_CH0	MT_CH1	MT_CH1N
36			PC9				MT_CH0									MT_CH0N		
37	25	21	PB2				MT_CH0N					SCTM0				MT_CH0	MT_CH1	CKIN
38	26	22	PB3				MT_CH0									MT_CH0N	MT_CH2N	MT_CH2
39			PB4				MT_CH2	SPI_SEL	UR_TX			SCTM3				MT_CH2N		
40			PB5					SPI_SCK										
41	27		PC1				MT_BRK0	SPI_MOSI	UR_RX		CMP1O	SCTM0						
42	28	23	PC2		ADC_IN0		MT_CH3	SPI_MISO				SCTM1						
43	29	24	PC3		ADC_IN1		GT_CH3				CMP1N							
44	30	1	PB6		ADC_IN2		GT_CH2			I2C_SCL	CMP1P2	SCTM2						
45	31	2	PB7		ADC_IN3		GT_CH1			I2C_SDA	CMP1P1							
46	32	3	PB8		ADC_IN4		GT_CH0		UR_TX		CMP1P0	SCTM3						
47			PC10				MT_BRK0			I2C_SCL		SCTM0						
48			PC11				MT_CH3			I2C_SDA		SCTM2						

Table 4. Pin Description

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP	32 QFN	24 SSOP					Default Function (AF0)
1	1		PA0	AI/O	5V	4/8/12/16 mA	PA0
2	2	4	PA1	AI/O	5V	4/8/12/16 mA	PA1
3	3	5	PA2	AI/O	5V	4/8/12/16 mA	PA2
4	4	6	PA3	AI/O	5V	4/8/12/16 mA	PA3
5	5		PA4	AI/O	5V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
6			PA5	AI/O	5V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
7	6	7	PA6	AI/O	5V	4/8/12/16 mA	PA6
8	7	8	PA7	AI/O	5V	4/8/12/16 mA	PA7
9	8	9	PC4	AI/O	5V	4/8/12/16 mA	PC4
10			PC5	AI/O	5V	4/8/12/16 mA	PC5
11			PC6	AI/O	5V	4/8/12/16 mA	PC6
12			PC7	AI/O	5V	4/8/12/16 mA	PC7
13	9	10	CLDO	P	—	—	Core power LDO V_{CORE} output A 2.2 μF capacitor must be connected as close as possible between this pin and VSS
14	10	11	VDD/ VDDA	P	—	—	Digital and analog voltage input
15	11	12	VSS/ VSSA	P	—	—	Ground reference
16	12	13	nRST(3)	I	5V_PU	—	External reset pin
17			PB9(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB9
18			PB10(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB10
19			PB11(3)	I/O (V_{DD})	5V	4/8/12/16 mA	PB11
20			PB12(3)	I/O (V_{DD})	5V	4/8/12/16 mA	LSTMOUT
21	13		PB13	AI/O	5V	4/8/12/16 mA	XTALIN
22	14		PB14	AI/O	5V	4/8/12/16 mA	XTALOUT
23			PB15	I/O	5V	4/8/12/16 mA	PB15
24			PC0	I/O	5V	4/8/12/16 mA	PC0
25	15		PA8	I/O	5V	4/8/12/16 mA	PA8
26	16	14	PA9	I/O	5V_PU	4/8/12/16 mA	PA9_BOOT
27	17		PA10	I/O	5V	4/8/12/16 mA	PA10
28	18		PA11	I/O	5V	4/8/12/16 mA	PA11
29	19	15	PA12	I/O	5V_PU	4/8/12/16 mA	SWCLK
30	20	16	PA13	I/O	5V_PU	4/8/12/16 mA	SWDIO
31	21	17	PA14	I/O	5V	4/8/12/16 mA	PA14
32	22	18	PA15	I/O	5V	4/8/12/16 mA	PA15
33	23	19	PB0	I/O	5V	4/8/12/16 mA	PB0
34	24	20	PB1	I/O	5V	4/8/12/16 mA	PB1
35			PC8	I/O	5V	4/8/12/16 mA	PC8

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
48 LQFP	32 QFN	24 SSOP					Default Function (AF0)
36			PC9	I/O	5V	4/8/12/16 mA	PC9
37	25	21	PB2	I/O	5V	4/8/12/16 mA	PB2
38	26	22	PB3	I/O	5V	4/8/12/16 mA	PB3
39			PB4	I/O	5V	4/8/12/16 mA	PB4
40			PB5	I/O	5V	4/8/12/16 mA	PB5
41	27		PC1	AI/O	5V	4/8/12/16 mA	PC1
42	28	23	PC2	AI/O	5V	4/8/12/16 mA	PC2
43	29	24	PC3	AI/O	5V	4/8/12/16 mA	PC3
44	30	1	PB6	AI/O	5V	4/8/12/16 mA	PB6
45	31	2	PB7	AI/O	5V	4/8/12/16 mA	PB7
46	32	3	PB8	AI/O	5V	4/8/12/16 mA	PB8
47			PC10	I/O	5V	4/8/12/16 mA	PC10
48			PC11	I/O	5V	4/8/12/16 mA	PC11

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 5V = 5 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 5.5	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 5.5	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	105	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.5	5.0	5.5	V
V_{DDA}	Analog Operating Voltage	—	2.5	5.0	5.5	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	$V_{DD} \geq 2.5$ V Regulator input @ I_{LDO} = 35 mA and voltage variation = ±5 %, After trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.5 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

Table 8. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	16.76	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 60 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	7.54	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	13.9	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 40 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	7.69	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	6.56	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 20 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	3.44	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	2.69	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 8 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	1.43	—	mA
		V_{DD} = 5.0 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals enabled	—	34.6	—	μA
		V_{DD} = 5.0 V, HSI off, PLL off, LSI on, f_{HCLK} = 32 kHz, f_{PCLK} = 32 kHz, all peripherals disabled	—	29.6	—	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Sleep Mode)	V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals enabled	—	11.22	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 60 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 60 MHz, all peripherals disabled	—	1.19	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals enabled	—	7.63	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 40 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 40 MHz, all peripherals disabled	—	0.94	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals enabled	—	4.16	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL = 20 MHz, f_{HCLK} = 0 MHz, f_{PCLK} = 20 MHz, all peripherals disabled	—	0.73	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals enabled	—	1.72	—	mA
		V_{DD} = 5.0 V, HSI = 8 MHz, PLL off, f_{HCLK} = 0 MHz, f_{PCLK} = 8 MHz, all peripherals disabled	—	0.35	—	mA
	Supply Current (Deep-Sleep Mode)	V_{DD} = 5.0 V, all clock off (HSE/HSI), LDO in low power mode, LSI on, LSTM on	—	25	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSI means 32 kHz low speed internal oscillator.
3. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 9. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 105 °C	2.22	2.35	2.48	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})		2.09	2.20	2.33	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 5.0 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 10. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown-Out Detection	After factory-trimmed V_{DD} Falling edge		2.37	2.45	2.53	V
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	2.57	2.65	2.73	V
			LVDS = 001	2.77	2.85	2.93	V
			LVDS = 010	2.97	3.05	3.13	V
			LVDS = 011	3.17	3.25	3.33	V
			LVDS = 100	3.37	3.45	3.53	V
			LVDS = 101	4.15	4.25	4.35	V
			LVDS = 110	4.35	4.45	4.55	V
			LVDS = 111	4.55	4.65	4.75	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 5.0 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 5.0 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 5.0 V	—	—	—	—	ms
I_{DDLVD}	Operation Current (3)	V_{DD} = 5.0 V	—	—	10	20	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 11. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	2.5	—	5.5	V
f_{HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 5.0 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	0.5	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 5.0 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 5.0 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 5.0 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 5.0 V	—	—	4	ms

Internal Clock Characteristics

Table 12. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 105 °C	2.5	—	5.5	V
f_{HSI}	HSI Frequency	V_{DD} = 5.0 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 5.0 V, T_A = 25 °C	-2	—	+2	%
		V_{DD} = 2.5 V ~ 5.5 V, T_A = -20 °C ~ 85 °C	-3	—	+3	%
		V_{DD} = 2.5 V ~ 5.5 V, T_A = 85 °C ~ 105 °C or T_A = -40 °C ~ -20 °C	-3.5	—	+3.5	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	Power Down Current		—	—	0.05	
t_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 8 MHz	—	—	10	μs

Table 13. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	2.5	—	5.5	V
f_{LSI}	LSI Frequency	V_{DD} = 5.0 V, T_A = -40 °C ~ 105 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 5.0 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 5.0 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 5.0 V, T_A = 25 °C	—	—	100	μs

System PLL Characteristics

Table 14. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	System PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	System PLL Output Clock	—	16	—	60	MHz
t_{LOCK}	System PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 15. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/ Erase Cycles before failure (Endurance)	T_A = -40 °C ~ 105 °C	10	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 105 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 105 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 105 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 105 °C	10	—	—	ms

I/O Port Characteristics

Table 16. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	5.0 V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	5.0 V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	5.0 V I/O		-0.5	—	0.35 × V_{DD}	V
		Reset pin		-0.5	—	0.35 × V_{DD}	
V_{IH}	High Level Input Voltage	5.0 V I/O		0.65 × V_{DD}	—	V_{DD} + 0.5	V
		Reset pin		0.65 × V_{DD}	—	V_{DD} + 0.5	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	5.0 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	
I_{OL}	Low Level Output Current (GPIO Sink Current)	5.0 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		5.0 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	mA
		5.0 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	mA
		5.0 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	mA
		V_{DD} Domain I/O drive @ V_{DD} = 5.0 V, V_{OL} = 0.4 V, PB9, PB10, PB11, PB12		4	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	5.0 V I/O 4 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		4	—	—	mA
		5.0 V I/O 8 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		8	—	—	mA
		5.0 V I/O 12 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		12	—	—	mA
		5.0 V I/O 16 mA drive, $V_{OH} = V_{DD}$ - 0.4 V		16	—	—	mA
		V_{DD} Domain I/O drive @ V_{DD} = 5.0 V, $V_{OH} = V_{DD}$ - 0.4 V, PB9, PB10, PB11, PB12		—	—	2	mA
V_{OL}	Low Level Output Voltage	5.0 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		5.0 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	
		5.0 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	
		5.0 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	
V_{OH}	High Level Output Voltage	5.0 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		5.0 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	
		5.0 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.4	—	—	
		5.0 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	5.0 V I/O, V_{DD} = 5.0 V		—	60	—	kΩ

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{PD}	Internal Pull-down Resistor	5.0 V I/O, V_{DD} = 5.0 V	—	60	—	kΩ

ADC Characteristics

Table 17. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	A/D Converter Operating Voltage	—	2.5	5.0	5.5	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	A/D Converter Operating Current	V_{DDA} = 5.0 V	—	0.85	1	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 5.0 V	—	—	0.1	µA
f_{ADC}	A/D Converter Clock Frequency	—	0.7	—	32	MHz
f_S	Sampling Rate	—	0.05	—	2	MHz
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	µs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	—	±2	LSB
DNL	Differential Non-linearity Error	f_S = 750 kHz, V_{DDA} = 5.0 V	—	—	±1	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

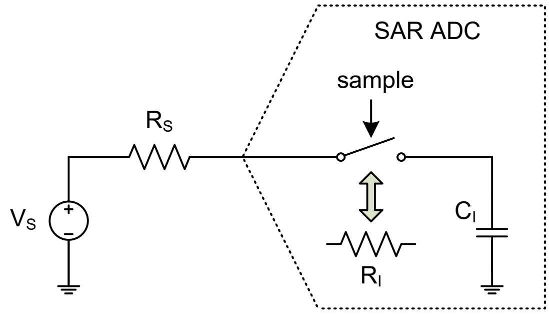


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Comparator Characteristics

Table 18. Comparator Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	Comparator mode		2.5	5.0	5.5	V
V_{IN}	Input Common Mode Voltage Range	CP or CN		V_{SSA}	—	V_{DDA}	V
V_{IOS}	Input Offset Voltage(1)	—		-15	—	15	mV
V_{HYS}	Input Hysteresis V_{DDA} = 5.0 V	No hysteresis, CMPHM [1:0] = 00		—	0	—	mV
		Low hysteresis, CMPHM [1:0] = 01		—	30	—	mV
		Middle hysteresis, CMPHM [1:0] = 10		—	60	—	mV
		High hysteresis, CMPHM [1:0] = 11		—	100	—	mV
t_{RT}	Response Time Input Overdrive = ±100 mV	High Speed Mode	$V_{DDA} \geq 2.7$ V	—	50	100	ns
			$V_{DDA} < 2.7$ V	—	100	250	ns
		Low Speed Mode		—	2	5	μs
I_{CMP}	Current Consumption V_{DDA} = 5.0 V	High Speed Mode		—	180	—	μA
		Low Speed Mode		—	30	—	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{CMPST}	Comparator Startup Time	Comparator enabled to output valid	—	—	50	μs
I_{CMP_DN}	Power Down Supply Current	CMPEN = 0 CVREN = 0 CVROE = 0	—	—	0.1	μA
Comparator Voltage Reference (CVR)						
V_{CVR}	Output Range	—	V_{SSA}	—	V_{DDA}	V
N_{Bits}	CVR Scaler Resolution	—	—	8	—	bits
t_{CVRST}	Settling Time	CVR Scaler Settling Time from CVRVAL = "00000000" to "11111111"	—	—	100	μs
I_{CVR}	Current Consumption V_{DDA} = 5.0 V	CVREN = 1, CVROE = 0	—	65	—	μA
		CVREN = 1, CVROE = 1	—	80	110	μA

Note: Data based on characterization results only, not tested in production.

Operational Amplifier Characteristics

Table 19. Operational Amplifier Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	OPA mode	3.0	5.0	5.5	V
I_{OPA_DN}	Power Down Current	—	—	—	0.1	μA
I_{OPA}	Operating Current	V_{DD} = 5V	—	800	—	μA
V_{OS}	Input Offset Voltage	Without calibration (OOF[4:0] = 10000B)	-15	—	15	mV
		With calibration	-2	—	2	mV
V_{OR}	Maximum Output Voltage Range	—	V_{SS} + 0.2	—	V_{DD} - 0.2	V
I_{OS}	Input Offset Current	$V_{IN} = 1/2V_{CM}$	—	1	10	nA
PSRR	Power Supply Rejection Ratio	—	—	60	—	dB
CMRR	Common Mode Rejection Ratio	V_{CM} = 0 ~ V_{DD} - 1.4	—	60	—	dB
SR	Slew Rate+, Slew Rate-	R_L = 100kΩ, C_L = 50pF	—	6	—	V/μs
GBW	Gain Band Width	R_L = 100kΩ, C_L = 50pF	—	6	—	MHz
A_{OL}	Open Loop Gain	R_L = 100kΩ, C_L = 50pF	60	80	—	dB
PM	Phase Margin	R_L = 100kΩ, C_L = 50pF	50	60	—	Deg
V_{CM}	Common Mode Voltage Range	—	V_{SS}	—	V_{DD} - 1.4	V

MCTM/GPTM/SCTM Characteristics

Table 20. MCTM/GPTM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for MCTM, GPTM and SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 21. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time	0	—	0	—	0	—	ns
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: SEQFILTER = 01 and COMBFILTEREN=0 that COMB filter is disabled.

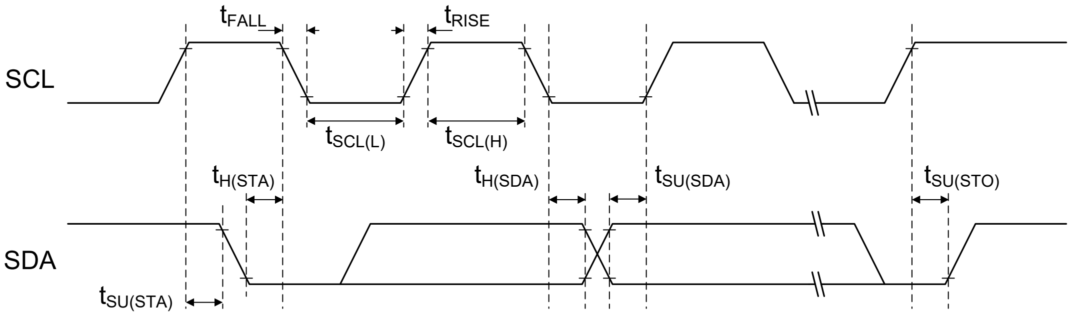


Figure 8. I²C Timing Diagram

SPI Characteristics

Table 22. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

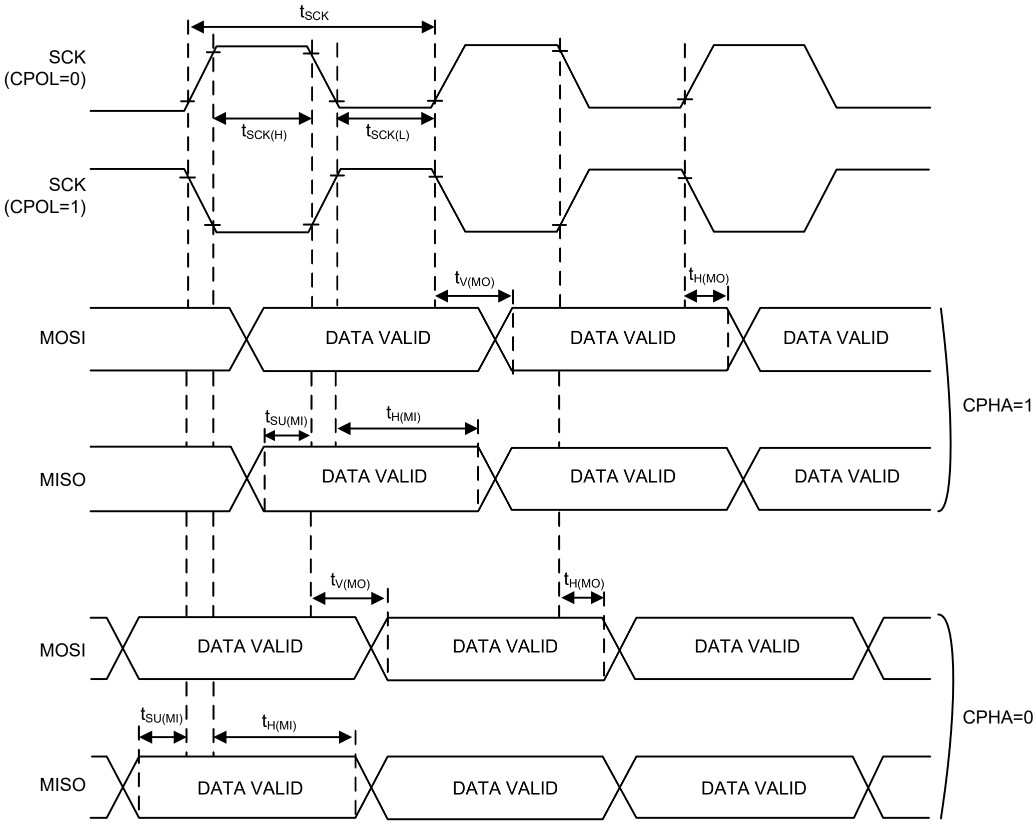


Figure 9. SPI Timing Diagram – SPI Master Mode

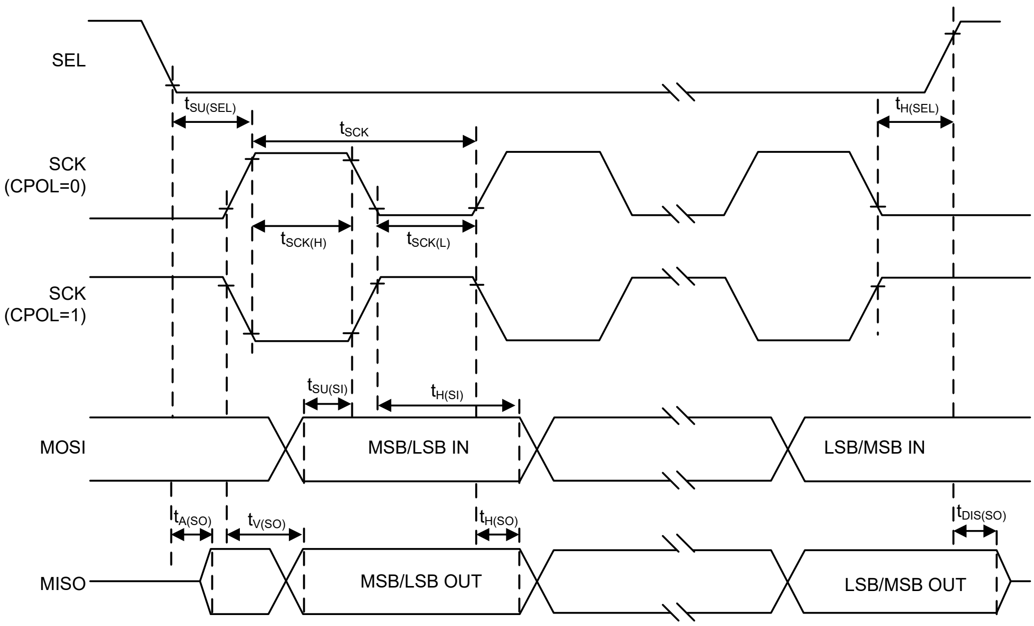


Figure 10. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

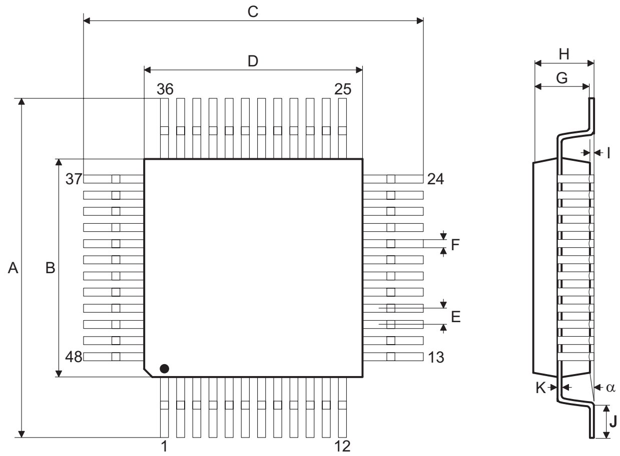
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

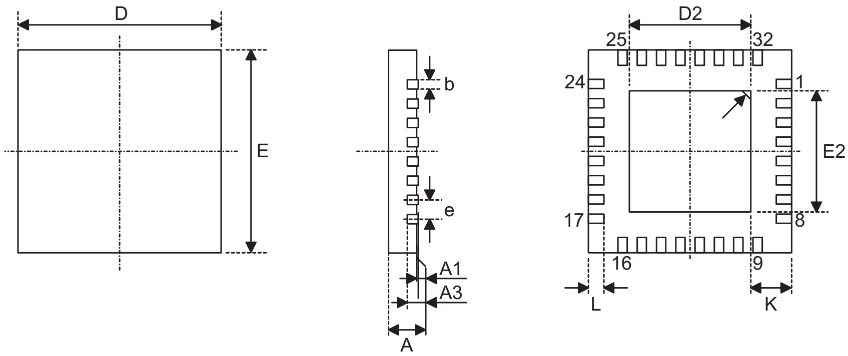
48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

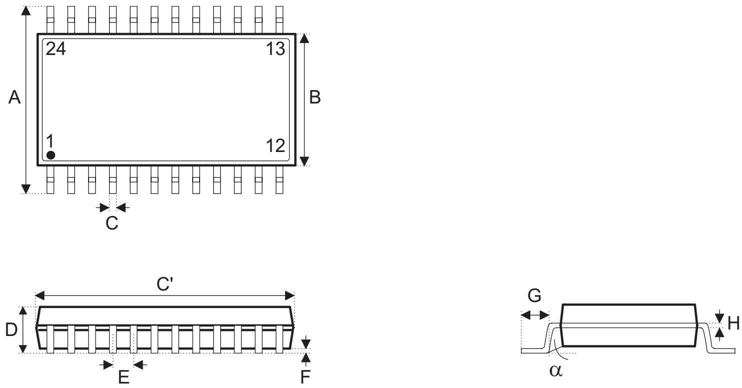
SAW Type 32-pin QFN (4mm × 4mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.157 BSC	—
E	—	0.157 BSC	—
e	—	0.016 BSC	—
D2	0.104	0.106	0.108
E2	0.104	0.106	0.108
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 BSC	—
b	0.15	0.20	0.25
D	—	4.00 BSC	—
E	—	4.00 BSC	—
e	—	0.40 BSC	—
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
K	0.20	—	—

24-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.008	—	0.012
C’	—	0.341 BSC	—
D	—	—	0.069
E	—	0.025 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.000 BSC	—
B	—	3.900 BSC	—
C	0.20	—	0.30
C’	—	8.660 BSC	—
D	—	—	1.75
E	—	0.635 BSC	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°