HT32F12364
Datasheet

32-Bit Arm® Cortex®-M3 Microcontroller,
256 KB Flash and 128 KB SRAM with 1 MSPS ADC,
USART, UART, SPI, I^2C, GPTM, PWM, SCTM, BFTM, PDMA,
CRC, SCI, RTC, WDT, AES, EBI and USB2.0 FS

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1 General Description

The Holtek HT32F12364 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M3 processor core. The Cortex®-M3 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and includes advanced debug support.

The device operates at a frequency of up to 72 MHz with a Flash accelerator to obtain maximum efficiency. It provides 256 KB of embedded Flash memory for code/data storage and 128 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, UART, SPI, SCI, PDMA, GPTM, PWM, SCTM, EBI, CRC-16/32, AES-128/256, USB2.0 FS and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition, smart door lock and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M3 processor core
- Up to 72 MHz operating frequency
- Single-cycle multiplication and hardware division
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many special features such as a Thumb-2 instruction set, hardware divider, low latency interrupt respond time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets.

On-Chip Memory

- 256 KB on-chip Flash memory for instruction/data and option storage
- 128 KB on-chip SRAM
- Supports multiple booting modes

The Arm® Cortex®-M3 processor is structured using Harvard architecture which uses a separate bus structure to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex®-M3 is 4 GB due to its 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M3 processor to reduce the software complexity of repeated implementation for different device vendors. However, some regions are used by the Arm® Cortex®-M3 system peripherals. Refer to the Arm® Cortex®-M3 Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the HT32F12364 device, including Code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word programming/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±1.5 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL and USB PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), an HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M3 are derived from the system clock (CK_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management Unit– PWRCU

- Single V_{DD} power supply: 1.65 V to 3.6 V
- Integrated 1.5 V LDO regulator for CPU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD} and 1.5 V
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 8 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 8 external analog signal channels and 3 internal channels can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference (V_{REF}) which can provide a stable reference voltage for the A/D Converter is internally connected to the ADC_BUILT-IN input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

I/O Ports – GPIO

- Up to 52 GPIOs
- Port A, B, C, D, F are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have configurable output driving current

There are up to 52 General Purpose I/O pins, GPIO, named from PA0~PA15 to PD0~PD2 and PF0 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up/down auto-reload counter
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Pulse-Width-Modulation Timer – PWM

- 16-bit up/down auto-reload counter
- Up to 4 independent channels for each timer
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output

The Pulse-Width-Modulation Timer, PWM, consists of one 16-bit up/down-counter, four 16-bit Compare Registers (CRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer and output waveform generation such as single pulse generation or PWM output.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned
- Single Pulse Mode Output

The Single Channel Timer, SCTM, consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM outputs.

Basic Function Timer – BFTM

- 32-bit compare/match count-up counters – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shot or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down-counter with a 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT counter value register, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. The Watchdog Timer can be operated in a reset mode. The Watchdog Timer will generate a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode or the three sleep modes. There is a register write protection function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real Time Clock – RTC

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC for short, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} Domain except for the APB interface. The APB interface is located in the V_{DDI5} power domain. Therefore, it is necessary to be isolated by the ISO signal that comes from the power control unit when the V_{DDI5} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the MCU power saving modes.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detection and clock synchronization function to prevent the situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to (f_{PCLK}/2) MHz for master mode and (f_{PCLK}/3) MHz for slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate clock frequency of up to (f_{PCLK}/16) MHz and synchronous operating baud rate clock frequency of up to (f_{PCLK}/8) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes an 8-level transmitter FIFO, (TX FIFO) and an 8-level receiver FIFO (RX FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency of up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard
- Character Transfer mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (Elementary Time Unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and check functions
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface, SCI, is compatible with the ISO 7816-3 standard. This interface includes functions for Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform the required Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16} + X^{15} + X^2 + 1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16} + X^{12} + X^5 + 1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Supports 1's complement, byte reverse and bit reverse operation on data and checksum
- Supports byte, half-word and word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports Linear address, circular address and fixed address modes

- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:
  ADC, SPI, USART, UART, I²C, SCI, GPTM, PWM, AES and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

External Bus Interface – EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Individual chip select signal for per memory bank
- Programmable timing to support a wide range of devices
- Automatic translation when AHB transaction width and external memory interface width is different
- Write buffer to decrease the stalling of the AHB write burst transaction
- Multiplexed and non-multiplexed address and data line configurations
  - Up to 21 address lines
  - Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the CPU internal address map. The data and address lines are multiplexed in order to reduce the number of pins required to connect to the external devices. The read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8-bit or 16-bit bus interface.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1024-byte EP_SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte EP_SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize overall system complexity and cost. The USB also contains suspend and resume features to meet low-power consumption requirement.

Advanced Encryption Standard – AES

- Supports AES Encrypt / Decrypt Function
- Supports AES ECB/CBC/CTR mode
- Supports Key Size 128, 192 and 256 bits
- Supports 4 words Initial Vector for CBC and CTR mode
- 8 × 32 bits (Each IN and OUT FIFO Capacity) for 2 AES Data blocks
- Supports PDMA Interface
- Supports Word Data Swap Function

The AES core supports both encryption and decryption functions and supports 128-bit input data. It should be noted that hardware does not pad out any input data bits, therefore users need to do pad action by software at first.

Debug Support

- Serial Wire Debug Port SW-DP
- 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patches
- 4 comparators for hardware watchpoints
- 1-bit asynchronous trace for serial wire debug mode – TRACESWO

Package and Operation Temperature

- 40-pin QFN and 48 / 64-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F12364
Main Flash (KB)		255
Option Bytes Flash (KB)		1
SRAM (KB)		128
Timers	GPTM	1
	PWM	1
	SCTM	2
	BFTM	2
	RTC	1
	WDT	1
Communication	USB	1
	USART	1
	UART	2
	SPI	2
	I^2C	2
	SCI	1
PDMA		6 channels
AES		1
EBI		1
CRC		1
GPIO		Up to 52
EXTI		16
12-bit ADC		1
Number of channels		Max. 8 Channels
CPU frequency		Up to 72 MHz
Operating voltage		1.65 V ~ 3.6 V
Operating temperature		-40 °C ~ 85 °C
Package		40-pin QFN and 48 / 64-pin LQFP

Block Diagram

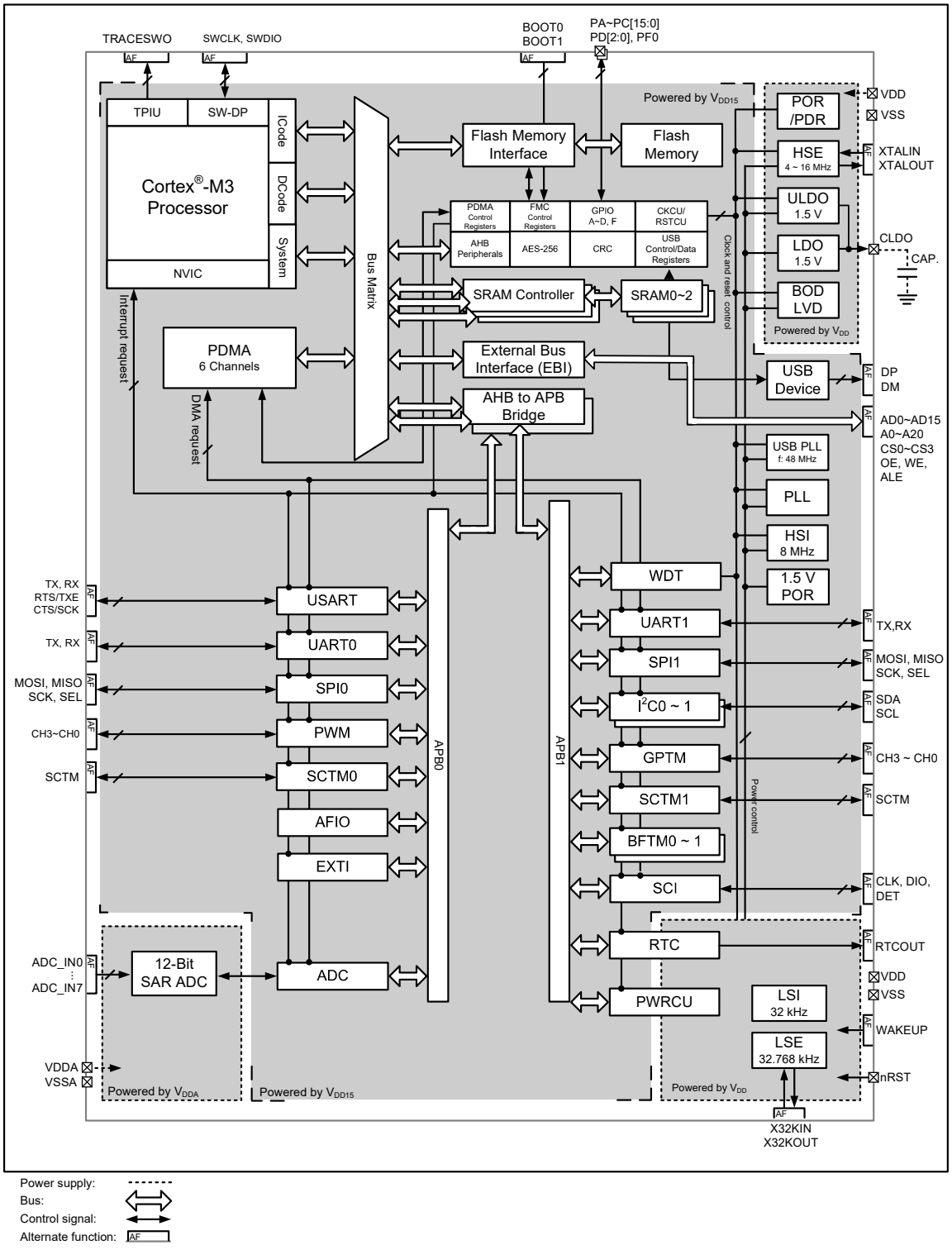


Figure 1. Block Diagram

Memory Map

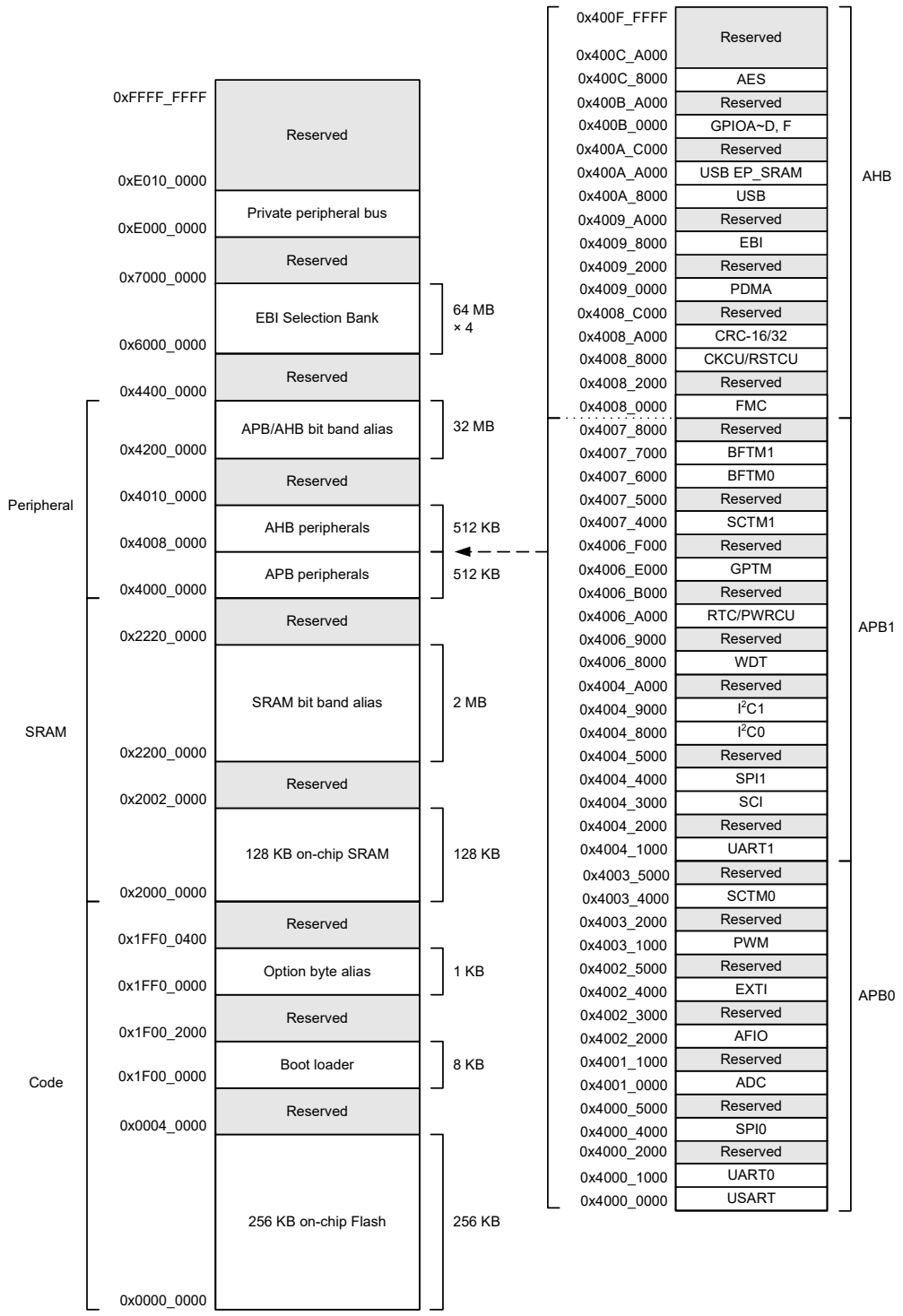


Figure 2. Memory Map

Table 2. HT32F12364 Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB0
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_0FFF	Reserved	
0x4003_1000	0x4003_1FFF	PWM	
0x4003_2000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_FFFF	Reserved	
0x4004_0000	0x4004_0FFF	Reserved	APB1
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	SCI	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC-16/32	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x4009_7FFF	Reserved	
0x4009_8000	0x4009_9FFF	EBI	
0x4009_A000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_9FFF	USB	
0x400A_A000	0x400A_BFFF	USB EP_SRAM	AHB
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	GPIOC	
0x400B_6000	0x400B_7FFF	GPIOD	
0x400B_8000	0x400C_9FFF	Reserved	
0x400B_A000	0x400B_BFFF	GPIOF	
0x400B_A000	0x400C_7FFF	Reserved	
0x400C_8000	0x400C_9FFF	AES	
0x400C_A000	0x400F_FFFF	Reserved	

Clock Structure

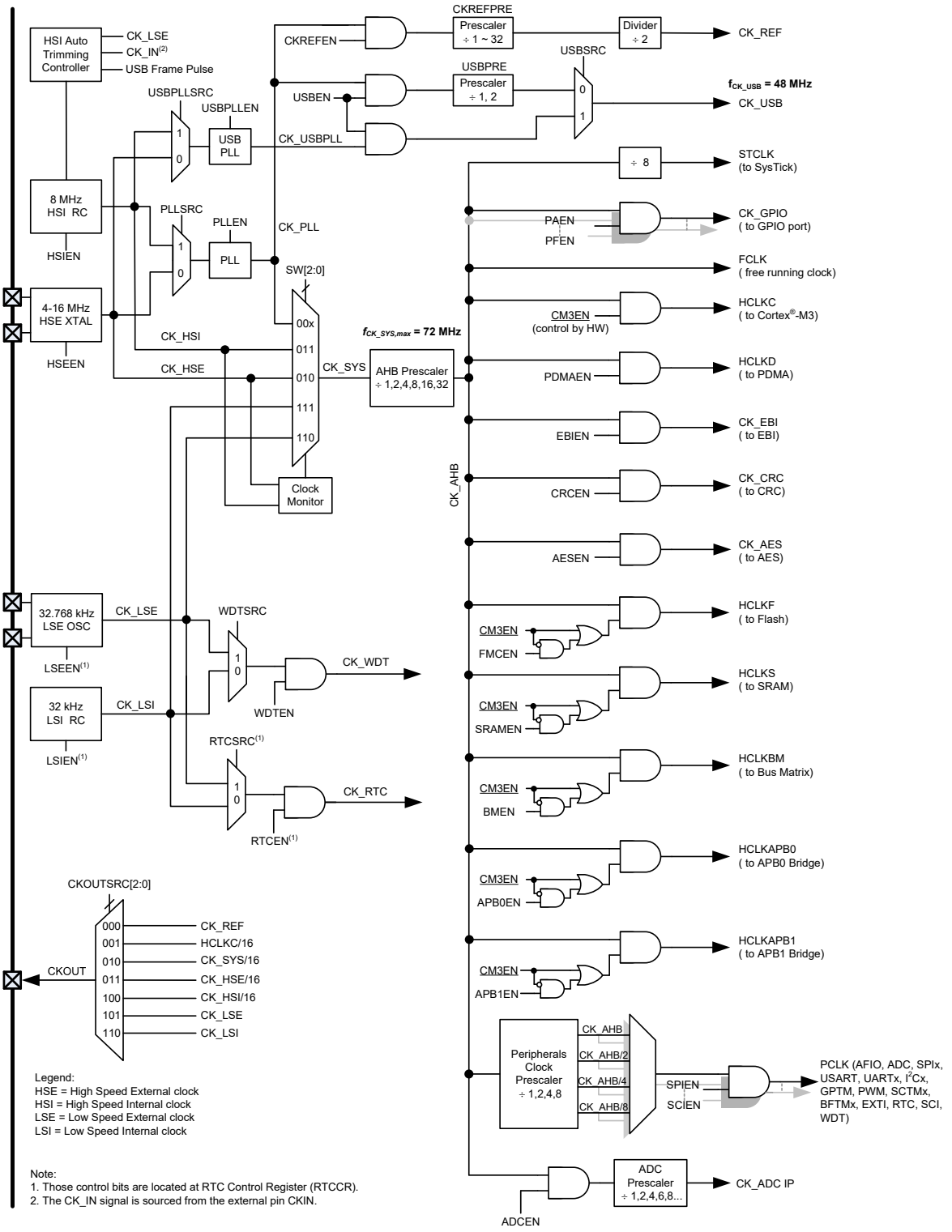


Figure 3. Clock Structure

4 Pin Assignment

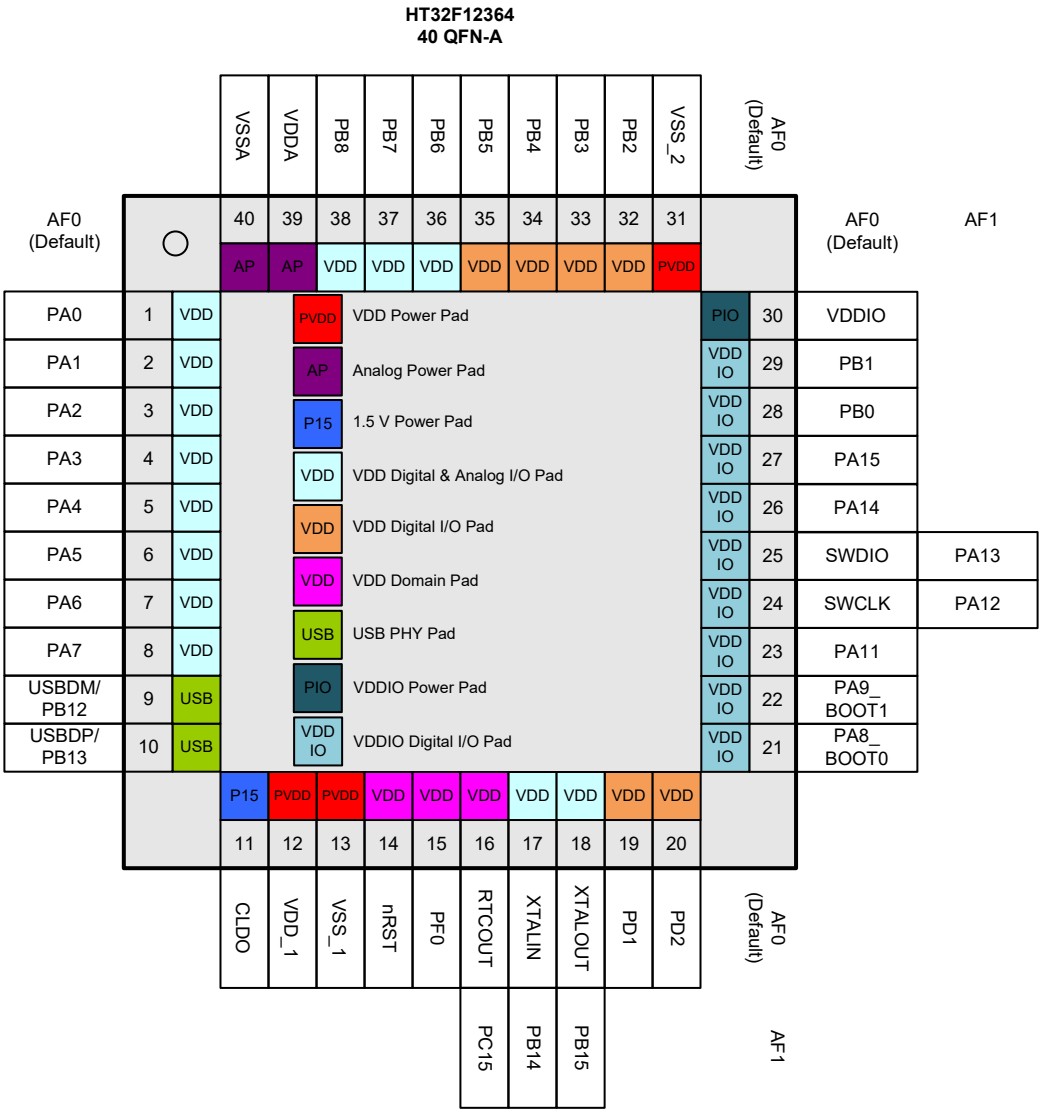


Figure 4. 40-pin QFN Pin Assignment

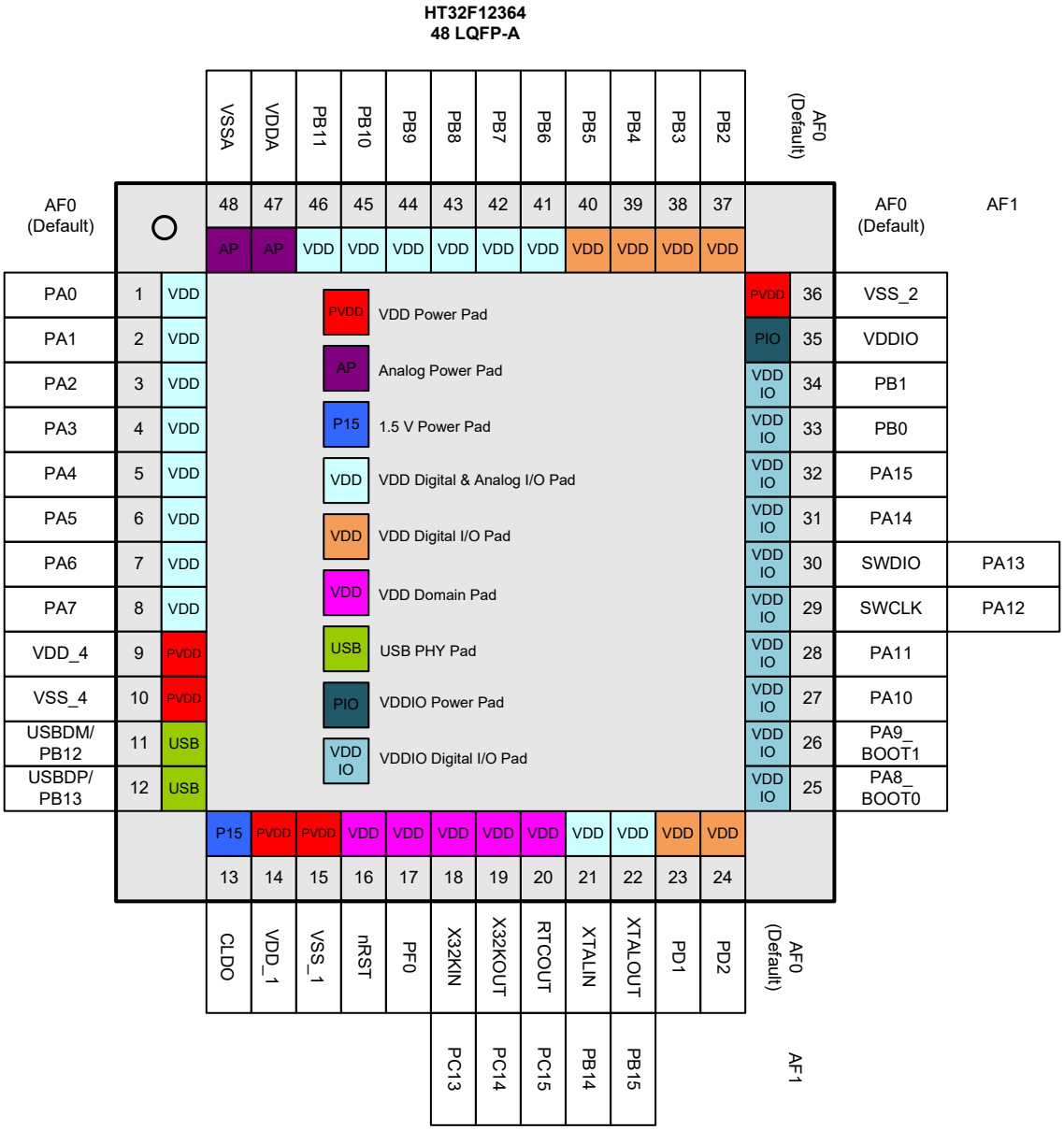


Figure 5. 48-pin LQFP Pin Assignment

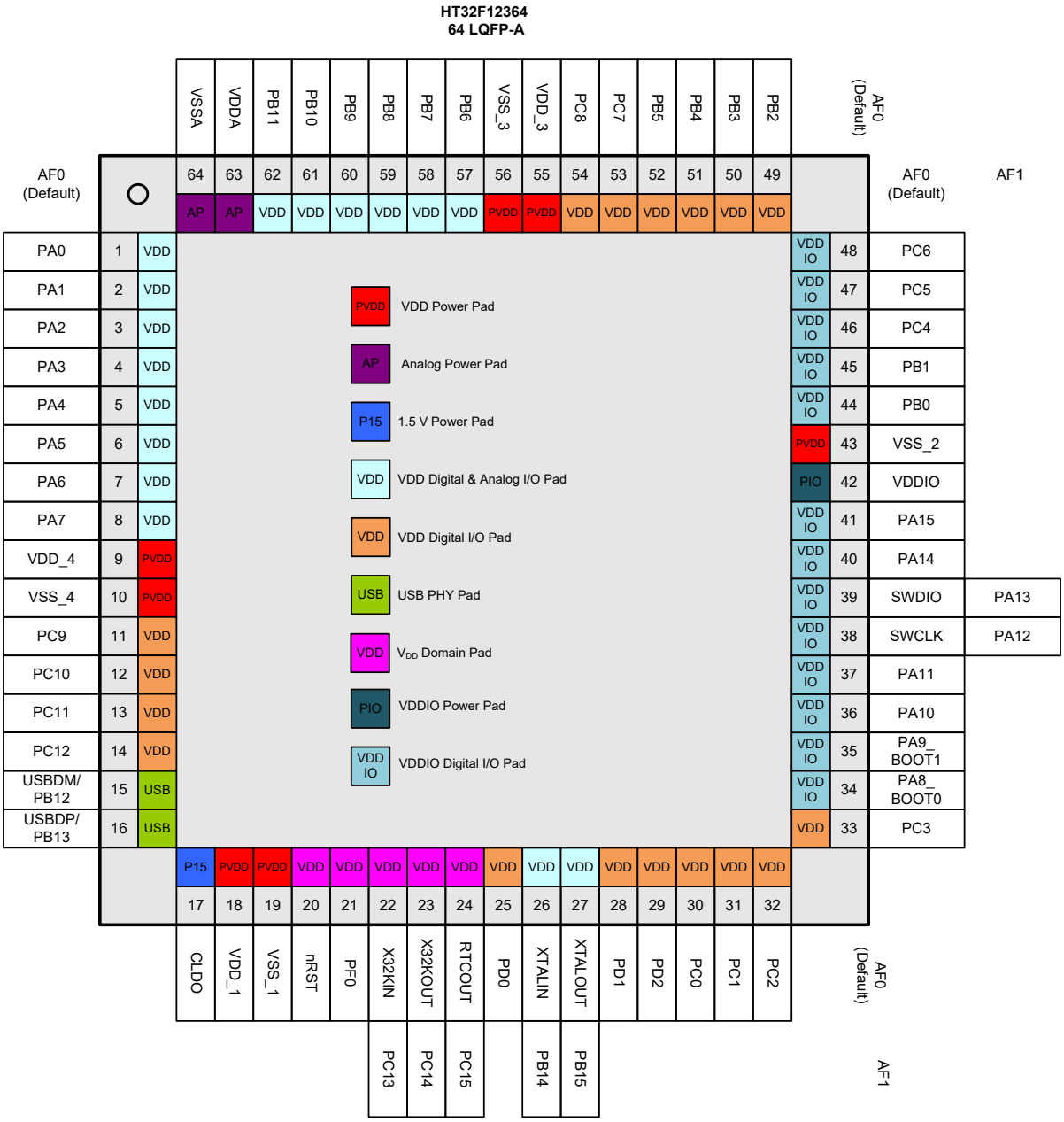


Figure 6. 64-pin LQFP Pin Assignment

Table 3. Pin Assignment

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	40 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	SCI	EBI	N/A	N/A	N/A	SCTM /PWM	N/A	System Other
1	1	1	PA0		ADC_IN0		GT_CH0	SPI1_SCK	USR_RTS	I2C1_SCL	SCI_CLK							VREF
2	2	2	PA1		ADC_IN1		GT_CH1	SPI1_MOSI	USR_CTS	I2C1_SDA	SCI_DIO							
3	3	3	PA2		ADC_IN2		GT_CH2	SPI1_MISO	USR_TX									
4	4	4	PA3		ADC_IN3		GT_CH3	SPI1_SEL	USR_RX									
5	5	5	PA4		ADC_IN4		GT_CH0	SPI0_SCK	USR_TX	I2C0_SCL	SCI_CLK							
6	6	6	PA5		ADC_IN5		GT_CH1	SPI0_MOSI	USR_RX	I2C0_SDA	SCI_DIO							
7	7	7	PA6		ADC_IN6		GT_CH2	SPI0_MISO	USR_RTS		SCI_DET							
8	8	8	PA7		ADC_IN7		GT_CH3	SPI0_SEL	USR_CTS									
9	9		VDD_4															
10	10		VSS_4															
11			PC9				GT_CH0	SPI1_SEL	UR0_TX	I2C1_SCL		EBI_A19						
12			PC10				GT_CH1	SPI1_SCK	UR0_RX	I2C1_SDA		EBI_A20						
13			PC11				GT_CH2	SPI1_MOSI				EBI_A0				SCTM0		
14			PC12				GT_CH3	SPI1_MISO				EBI_A1				SCTM1		
15	11	9	PB12						USR_TX	I2C0_SCL								
15	11	9	USBDM															
16	12	10	USBDP															
16	12	10	PB13						USR_RX	I2C0_SDA								
17	13	11	CLDO															
18	14	12	VDD_1															
19	15	13	VSS_1															
20	16	14	nRST															
21	17	15	PF0													PWM_CH1		
22	18		X32KIN	PC13			GT_CH0		USR_TX							SCTM0		
23	19		X32KOUT	PC14			GT_CH1		USR_RX							SCTM1		
24	20	16	RTCOUT	PC15					UR0_RX							PWM_CH0		WAKEUP
25			PD0							I2C0_SDA		EBI_A18				SCTM0		
26	21	17	XTALIN	PB14														
27	22	18	XTALOUT	PB15														
28	23	19	PD1					SPI0_SEL		I2C1_SCL	SCI_CLK	EBI_A16				PWM_CH2		
29	24	20	PD2					SPI0_SCK		I2C1_SDA	SCI_DIO	EBI_A17				PWM_CH3		
30			PC0				GT_CH0	SPI1_SEL				EBI_AD13						
31			PC1				GT_CH1	SPI1_SCK				EBI_AD14						
32			PC2				GT_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL		EBI_AD15				SCTM0		
33			PC3				GT_CH3	SPI1_MISO	UR1_RX	I2C0_SDA	SCI_DET	EBI_CS3				SCTM1		

Package			Alternate Function Mapping															
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64 LQFP	48 LQFP	40 QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I^2C	SCI	EBI	N/A	N/A	N/A	SCTM /PWM	N/A	System Other
34	25	21	PA8 _BOOT0				GT_ ETI		USR_TX		SCI_ CLK					PWM_ CH3		CKOUT
35	26	22	PA9 _BOOT1					SPI0_ MOSI			SCI_ DIO	EBI_ A1				PWM_ CH2		
36	27		PA10						USR_RX		SCI_ DET					PWM_ CH1		
37	28	23	PA11					SPI0_ MISO			SCI_ DET	EBI_ A0				SCTM0		TRACESWO
38	29	24	SWCLK	PA12														
39	30	25	SWDIO	PA13														
40	31	26	PA14					SPI1_ SEL	USR_TX		SCI_ CLK	EBI_ AD0				PWM_ CH0		
41	32	27	PA15					SPI1_ SCK	USR_RX		SCI_ DIO	EBI_ AD1				SCTM1		
44	33	28	PB0					SPI1_ MOSI	USR_TX	I2C0_ SCL		EBI_ AD2				PWM_ CH1		
45	34	29	PB1					SPI1_ MISO	USR_RX	I2C0_ SDA		EBI_ AD3				PWM_ CH3		
46			PC4						USR_ RTS		SCI_ CLK	EBI_ AD10						
47			PC5						USR_ CTS		SCI_ DIO	EBI_ AD11						
48			PC6								SCI_ DET	EBI_ AD12						
42	35	30	VDDIO															
43	36	31	VSS2															
49	37	32	PB2					SPI0_ SEL	UR0_TX			EBI_ AD4				PWM_ CH2		CKIN
50	38	33	PB3					SPI0_ SCK	UR0_RX			EBI_ AD5				SCTM1		
51	39	34	PB4					SPI0_ MOSI	UR1_TX			EBI_ AD6				SCTM0		
52	40	35	PB5				GT_ CH2	SPI0_ MISO	UR1_RX			EBI_ AD7						
53			PC7							I2C0_ SCL		EBI_ AD8						
54			PC8							I2C0_ SDA		EBI_ AD9				SCTM1		
55			VDD_3															
56			VSS_3															
57	41	36	PB6					SPI1_ SEL	UR1_TX			EBI_ OE				PWM_ CH0		
58	42	37	PB7					SPI1_ SCK				EBI_ CS0				PWM_ CH0		
59	43	38	PB8				GT_ ETI	SPI1_ MOSI	UR1_RX			EBI_ WE				PWM_ CH2		
60	44		PB9				GT_ CH3	SPI1_ MISO	UR0_TX		SCI_ CLK	EBI_ ALE						
61	45		PB10						UR0_TX	I2C1_ SCL	SCI_ DET	EBI_ CS1				PWM_ CH3		
62	46		PB11						UR0_RX	I2C1_ SDA	SCI_ DIO	EBI_ CS2				PWM_ CH1		
63	47	39	VDDA															
64	48	40	VSSA															

Table 4. Pin Description

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64 LQFP	48 LQFP	40 QFN					Default Function (AF0)
1	1	1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	2	2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	3	3	PA2	AI/O	33V	4/8/12/16 mA	PA2, this pin provides a UART_TX function in the Boot loader mode.
4	4	4	PA3	AI/O	33V	4/8/12/16 mA	PA3, this pin provides a UART_RX function in the Boot loader mode.
5	5	5	PA4	AI/O	33V	4/8/12/16 mA	PA4
6	6	6	PA5	AI/O	33V	4/8/12/16 mA	PA5
7	7	7	PA6	AI/O	33V	4/8/12/16 mA	PA6
8	8	8	PA7	AI/O	33V	4/8/12/16 mA	PA7
9	9		VDD_4	P	—	—	Voltage for V_{DD} domain digital I/O
10	10		VSS_4	P	—	—	Ground reference for digital I/O
11			PC9	I/O	33V	4/8/12/16 mA	PC9
12			PC10	I/O	33V	4/8/12/16 mA	PC10
13			PC11	I/O	33V	4/8/12/16 mA	PC11
14			PC12	I/O	33V	4/8/12/16 mA	PC12
15	11	9	PB12	I/O	33V	4/8/12/16 mA	PB12
15	11	9	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard
16	12	10	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard
16	12	10	PB13	I/O	33V	4/8/12/16 mA	PC7
17	13	11	CLDO	P	—	—	Core power LDO 1.5 V output. It must be connected with a 4.7 μF capacitor which should be as close as possible between this pin and VSS_1.
18	14	12	VDD_1	P	—	—	Voltage for V_{DD} domain digital I/O
19	15	13	VSS_1	P	—	—	Ground reference for digital I/O
20	16	14	nRST(3)	I (V_{DD})	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	17	15	PF0(3)	I/O (V_{DD})	33V	4/8/12/16 mA	PF0
22	18		PC13(3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
23	19		PC14(3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
24	20	16	PC15(3)	I/O (V_{DD})	33V	4/8/12/16 mA	RTCOUT
25			PD0	I/O	33V	4/8/12/16 mA	PD0
26	21	17	PB14	AI/O	33V	4/8/12/16 mA	XTALIN
27	22	18	PB15	AI/O	33V	4/8/12/16 mA	XTALOUT
28	23	19	PD1	I/O	33V	4/8/12/16 mA	PD1
29	24	20	PD2	I/O	33V	4/8/12/16 mA	PD2
30			PC0	I/O	33V	4/8/12/16 mA	PC0
31			PC1	I/O	33V	4/8/12/16 mA	PC1
32			PC2	I/O	33V	4/8/12/16 mA	PC2
33			PC3	I/O	33V	4/8/12/16 mA	PC3

Pin Number			Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64 LQFP	48 LQFP	40 QFN					Default Function (AF0)
34	25	21	PA8	I/O (V_{DDIO})	33V_PU	4/8/12/16 mA	PA8_BOOT0
35	26	22	PA9	I/O (V_{DDIO})	33V_PU	4/8/12/16 mA	PA9_BOOT1
36	27		PA10	I/O (V_{DDIO})	33V	4/8/12/16 mA	PA10
37	28	23	PA11	I/O (V_{DDIO})	33V	4/8/12/16 mA	PA11
38	29	24	PA12	I/O (V_{DDIO})	33V_PU	4/8/12/16 mA	SWCLK
39	30	25	PA13	I/O (V_{DDIO})	33V_PU	4/8/12/16 mA	SWDIO
40	31	26	PA14	I/O (V_{DDIO})	33V_PU	4/8/12/16 mA	PA14
41	32	27	PA15	I/O (V_{DDIO})	33V_PU	4/8/12/16 mA	PA15
42	35	30	VDDIO	P	—	—	Voltage for V_{DDIO} domain digital I/O
43	36	31	VSS_2	P	—	—	Ground reference for digital I/O
44	33	28	PB0	I/O (V_{DDIO})	33V	4/8/12/16 mA	PB0
45	34	29	PB1	I/O (V_{DDIO})	33V	4/8/12/16 mA	PB1
46			PC4	I/O (V_{DDIO})	33V	4/8/12/16 mA	PC4
47			PC5	I/O (V_{DDIO})	33V	4/8/12/16 mA	PC5
48			PC6	I/O (V_{DDIO})	33V	4/8/12/16 mA	PC6
49	37	32	PB2	I/O	33V	4/8/12/16 mA	PB2
50	38	33	PB3	I/O	33V	4/8/12/16 mA	PB3
51	39	34	PB4	I/O	33V	4/8/12/16 mA	PB4
52	40	35	PB5	I/O	33V	4/8/12/16 mA	PB5
53			PC7	I/O	33V	4/8/12/16 mA	PC7
54			PC8	I/O	33V	4/8/12/16 mA	PC8
55			VDD_4	P	—	—	Voltage for V_{DD} domain digital I/O
56			VSS_4	P	—	—	Ground reference for digital I/O
57	41	36	PB6	AI/O	33V	4/8/12/16 mA	PB6
58	42	37	PB7	AI/O	33V	4/8/12/16 mA	PB7
59	43	38	PB8	AI/O	33V	4/8/12/16 mA	PB8
60	44		PB9	AI/O	33V	4/8/12/16 mA	PB9
61	45		PB10	AI/O	33V	4/8/12/16 mA	PB10
62	46		PB11	AI/O	33V	4/8/12/16 mA	PB11
63	47	39	VDDA	P	—	—	Analog voltage for ADC
64	48	40	VSSA	P	—	—	Ground reference for the ADC

Note: 1. I = Input, O = Output, A = Analog port, P = Power supply, PU = Pull-up, V_{DD} = V_{DD} Power.
2. 33V = 3.3 V Operation I/O Type.
3. These pins are located at the V_{DD} power domain
4. In the Boot loader mode, the UART and USB interfaces are available for communication.

5 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDIO}	External I/O Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage on Other I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-55	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-4000	4000	V

Recommended DC Operating Conditions

Table 6. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	1.65	3.30	3.60	V
V_{DDIO}	I/O Operating Voltage	—	1.65	3.30	3.60	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 7. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{LDO} = 30 mA and voltage variant = ±5 %, after trimming	1.425	1.500	1.570	V
I_{LDO}	Output Current	V_{DD} = 1.65 V ~ 3.6 V Regulator input @ V_{LDO} = 1.5 V	—	50	75	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	2.2	4.7	—	μF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 8. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 1.65 V Regulator input @ I_{ULDO} = 2 mA and voltage variant = ±5 %, after trimming	1.425	1.500	1.570	V
I_{ULDO}	Output Current	V_{DD} = 1.65 V ~ 3.6 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1.0	2.2	—	μF

Power Consumption

Table 9. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Run Mode	72 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 72 MHz	All peripherals enabled	27.4	31.3	—	mA
				All peripherals disabled	16.5	18.9	—	
		60 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 60 MHz	All peripherals enabled	24.2	27.7	—	
				All peripherals disabled	15.0	17.1	—	
		40 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 40 MHz	All peripherals enabled	20.0	22.8	—	
				All peripherals disabled	13.7	15.7	—	
		8 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 48 MHz	All peripherals enabled	5.3	6.0	—	
				All peripherals disabled	3.2	3.7	—	
		32 kHz	V_{DD} = 3.3 V LSI = 32 kHz LDO off, ULDO on	All peripherals enabled	29.2	38.6	—	μA
				All peripherals disabled	23.7	31.4	—	

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Sleep Mode	72 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 72 MHz	All peripherals enabled	15.4	17.6	—	mA
				All peripherals disabled	1.9	2.1	—	
		60 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 60 MHz	All peripherals enabled	13.0	14.9	—	
				All peripherals disabled	1.6	1.9	—	
		40 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 40 MHz	All peripherals enabled	9.0	10.2	—	
				All peripherals disabled	1.3	1.4	—	
		8 MHz	V_{DD} = 3.3 V HSI = 8 MHz PLL = 48 MHz	All peripherals enabled	2.7	3.1	—	
				All peripherals disabled	0.4	0.5	—	
	Deep-Sleep1 Mode	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		11.6	17.8	—	μA
	Deep-Sleep2 Mode	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		11.6	17.8	—	
	Power-Down Mode	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC on		1.30	1.99	—	
			V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC off		1.18	1.81	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 10. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.40	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO and ULDO will be turned off.

Table 11. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.80	
$V_{BODHYST}$	BOD Hysteresis	V_{DD} = 2.0 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	ms
I_{DDLVD}	Operation Current (3)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.
3. Bandgap current is not included.
4. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 12. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.60	V
f_{CK_HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V_{DD} = 2.5 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 13. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.60	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 1.65 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L \geq$ 7 pF, V_{DD} = 1.65 V ~ 2.7 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, $C_L <$ 7 pF, V_{DD} = 1.65 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	LSE Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 1.65 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace length as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the high frequency signal lines away from the crystal area to prevent the crosstalk adverse effects.

Internal Clock Characteristics

Table 14. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	T_A = -40 °C ~ 85 °C	1.65	—	3.60	V
f_{CK_HSI}	HSI Frequency	V_{DD} = 3.3 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V T_A = 25 °C	-1.5	—	1.5	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -20 °C ~ 60 °C	-2.5	—	2.5	%
		V_{DD} = 1.65 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-3	—	3	%
Duty	Duty Cycle	f_{CK_HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{CK_HSI} = 8 MHz	—	300	500	μA
	HSI Oscillator Power Down Current		—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{CK_HSI} = 8 MHz	—	—	10	μs

Table 15. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage Range	—	1.65	—	3.6	V
f_{CK_LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V, T_A = 25 °C	—	—	100	μs

PLL Characteristics

Table 16. PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	8	—	80	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

USB PLL Characteristics

Table 17. USB PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 18. Flash Memory Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	10	—	—	K cycles
T_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	V_I = V_{SS}, On-chip pull-up resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
I_{IH}	High Level Input Current	3.3 V I/O	V_I = V_{DD}, On-chip pull-down resistor disabled	—	—	3	μA
		Reset pin		—	—	3	
V_{IL}	Low Level Input Voltage	3.3 V I/O		- 0.4	—	V_{DD} × 0.35	V
		Reset pin		- 0.4	—	V_{DD} × 0.35	
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.4	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.4	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V	8	—	—	
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V	12	—	—	
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V	16	—	—	
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.4 V	8	—	—	
		3.3 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.4 V	12	—	—	
		3.3 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.4 V	16	—	—	
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA	—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA	—	—	0.4	
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA	—	—	0.4	
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA	—	—	0.4	
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	
		3.3 V 12 mA drive I/O, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	
R_{PU}	Internal Pull-up Resistor	3.3 V I/O, V_{DD} = 3.3 V	—	60	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O, V_{DD} = 3.3 V	—	60	—	kΩ

ADC Characteristics

Table 20. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{DDA}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	0.85	1.00	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock	—	0.7	—	16.0	MHz
f_S	Sampling Rate	—	0.05	—	1.00	MHz
T_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$T_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$T_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 kHz, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750 kHz, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S may not have an arbitrarily large value.

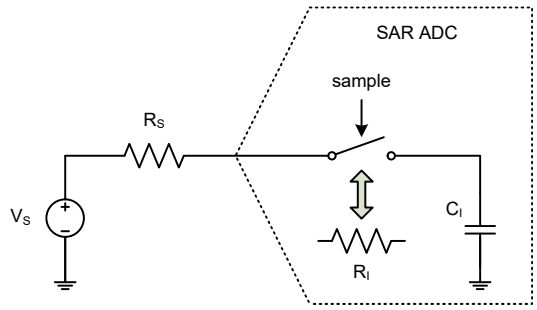


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

Internal Reference Voltage Characteristics

Table 21. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		1.8	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 °C Temperature	V_{DDA} ≥ 1.8 V	VREFSEL[1:0] = 00	1.190	1.215	1.240	V
		V_{DDA} ≥ 2.3 V	VREFSEL[1:0] = 01	1.96	2.00	2.04	
		V_{DDA} ≥ 2.8 V	VREFSEL[1:0] = 10	2.45	2.50	2.55	
		V_{DDA} ≥ 3.0 V	VREFSEL[1:0] = 11	2.65	2.70	2.75	
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 1.8 V ~ 3.6 V, V_{REF} = 1.215 V, T_A = -40 °C ~ 85 °C		-3.0	—	+3.0	%
t_{STABLE}	Reference Voltage Stable Time	—		—	—	100	ms
t_{SREFV}	ADC Sampling Time when Reading Reference Voltage	—		10	—	—	μs
I_{DD}	Operating Current	V_{DDA} = 3.3 V, V_{REF} = 2.0 V, T_A = -40 °C ~ 85 °C		—	45	55	μA
I_{DDPWD}	Reference Voltage Power Down Current	—		—	—	0.01	μA

V_{DDA} Monitor Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R	Resistor Bridge for V_{DDA}	—	—	50	—	kΩ
Q	Ratio on V_{DDA} Measurement	—	—	2	—	—
E_R	Error on Ratio	—	-1	—	+1	%
t_{SVDDA}	ADC Sampling Time when Reading the V_{DDA}	—	5	—	—	μs

Note: Guaranteed by design, not tested in production.

GPTM/PWM/SCTM Characteristics

Table 22. GPTM/PWM/SCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM, PWM and SCTM	—	—	—	f_{PCLK}	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Single Frequency on Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 23. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.500	—	1.125	—	0.450	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.500	—	1.125	—	0.450	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.300	—	0.340	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.300	—	0.340	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.600	—	0.475	—	0.250	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 0 and SEQ_FILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMB_FILTER_En = 1 and SEQ_FILTER = 00.

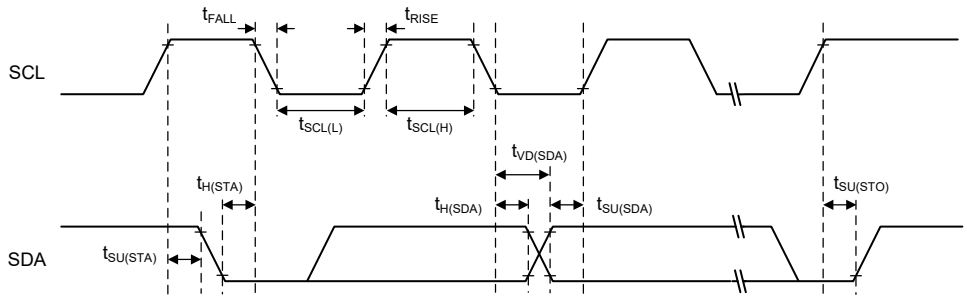


Figure 8. I²C Timing Diagram

SPI Characteristics

Table 24. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

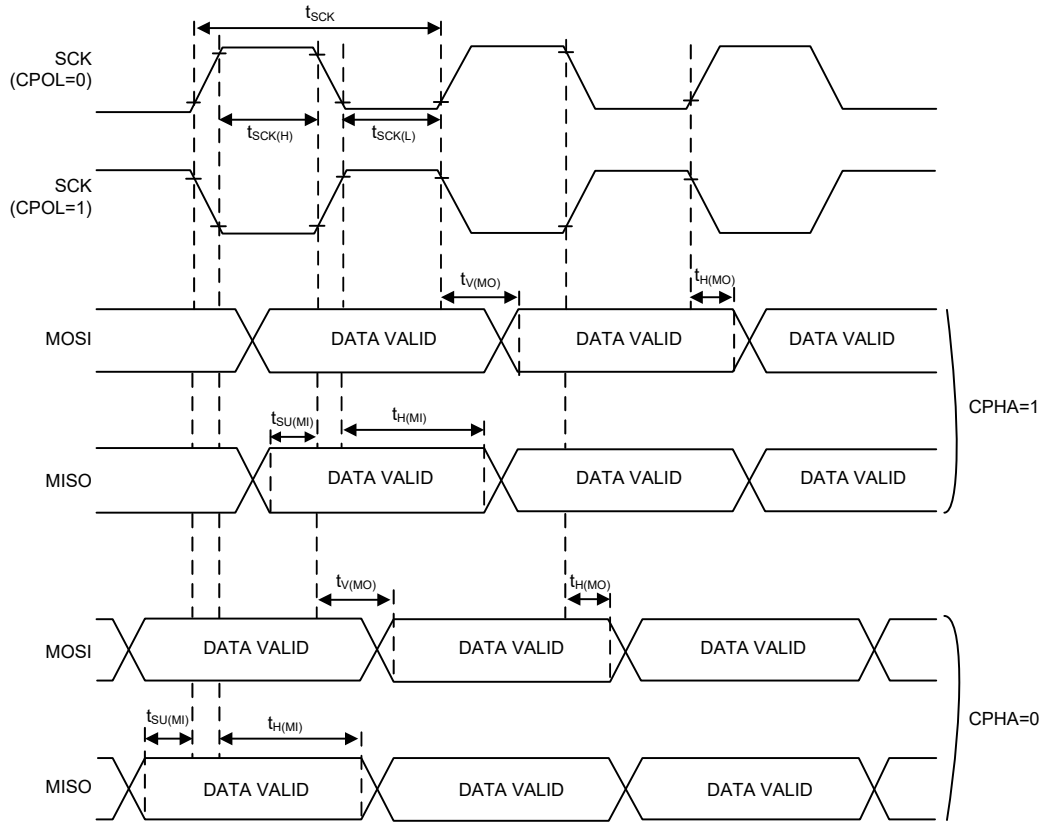


Figure 9. SPI Timing Diagram – SPI Master Mode

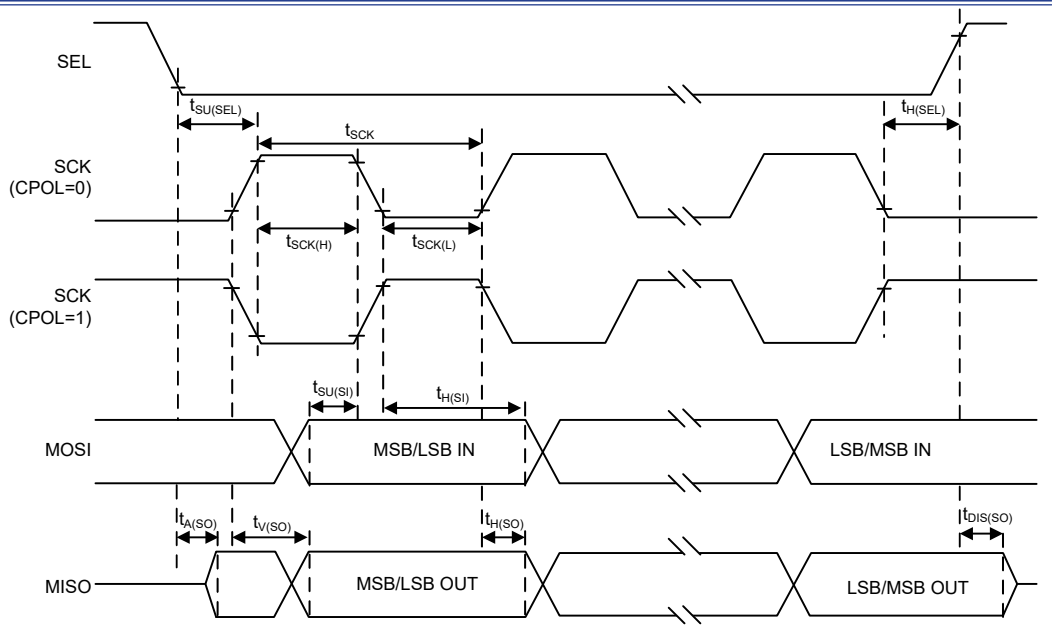


Figure 10. SPI Timing Diagram – SPI Slave Mode with CPHA = 1

USB Characteristics

The USB interface is USB-IF certified – Full Speed.

Table 25. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	USB Operating Voltage	—	3.0	—	3.6	V
V_{DI}	Differential Input Sensitivity	|USBDP – USBDM|	0.2	—	—	V
V_{CM}	Common Mode Voltage Range	—	0.8	—	2.5	V
V_{SE}	Single-ended Receiver Threshold	—	0.8	—	2.0	V
V_{OL}	Pad Output Low Voltage	R_L of 1.5 kΩ to V_{DD}	0	—	0.3	V
V_{OH}	Pad Output High Voltage		2.8	—	3.6	V
V_{CRS}	Differential Output Signal Cross-point Voltage		1.3	—	2.0	V
Z_{DRV}	Driver Output Resistance	—	—	10	—	Ω
C_{IN}	Transceiver Pad Capacitance	—	—	—	20	pF

Note: 1. Guaranteed by design, not tested in production.
2. The USB functionality is ensured down to 2.7 V but not for the full USB electrical characteristics which will experience degradation in the V_{DD} voltage range of 2.7 V to 3.0 V.
3. R_L is the resistor load connected to the USB driver USBDP.

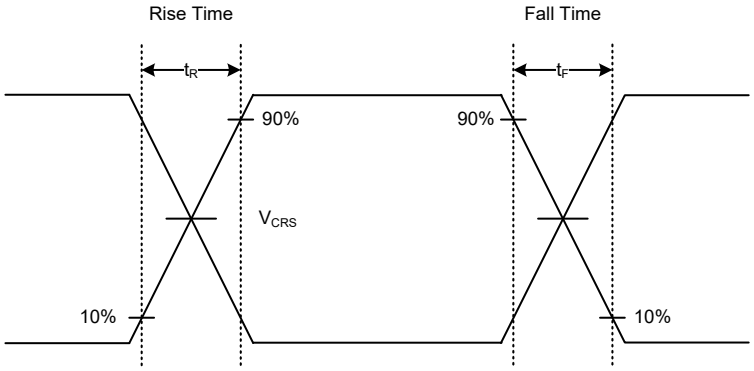


Figure 11. USB Signal Rise Time and Fall Time and Cross-Point Voltage (V_{CRS}) Definition

Table 26. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_r	Rise Time	C_L = 50 pF	4	—	20	ns
T_f	Fall Time	C_L = 50 pF	4	—	20	ns
$T_{r/f}$	Rise Time / Fall Time Matching	$T_{r/f} = T_r / T_f$	90	—	110	%

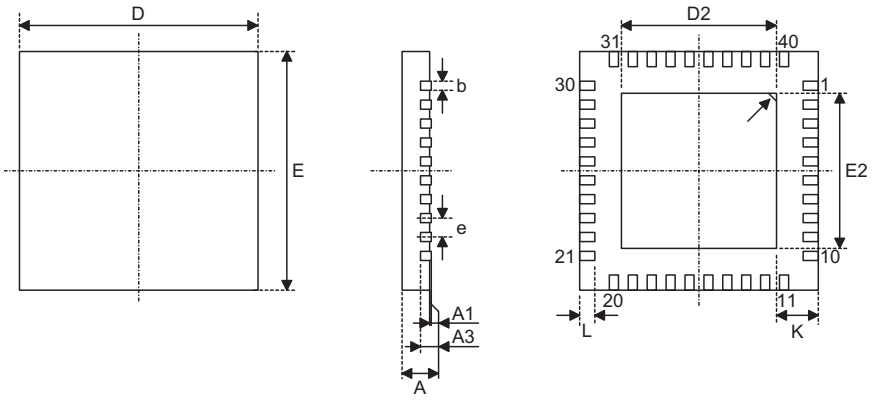
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consul

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

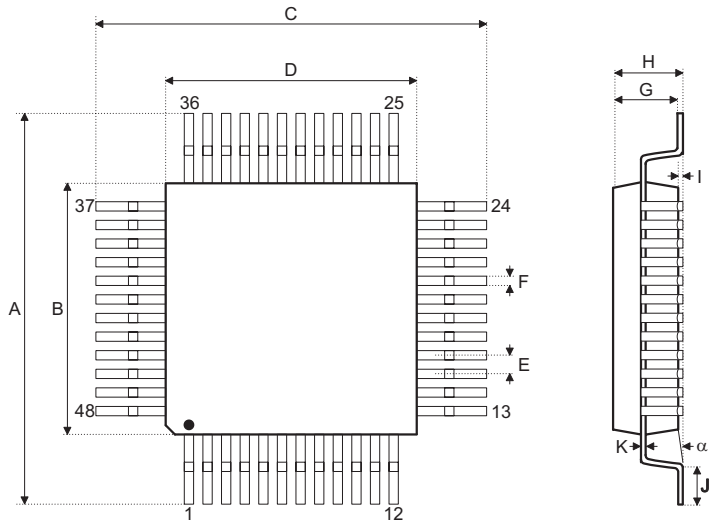
SAW Type 40-pin QFN (5mm × 5mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	—	0.197 BSC	—
E	—	0.197 BSC	—
e	—	0.016 BSC	—
D2	0.126	0.130	0.132
E2	0.126	0.130	0.132
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	—	0.200 BSC	—
b	0.150	0.200	0.250
D	—	5.000 BSC	—
E	—	5.000 BSC	—
e	—	0.40 BSC	—
D2	3.20	3.30	3.35
E2	3.20	3.30	3.30
L	0.35	0.40	0.45
K	0.20	—	—

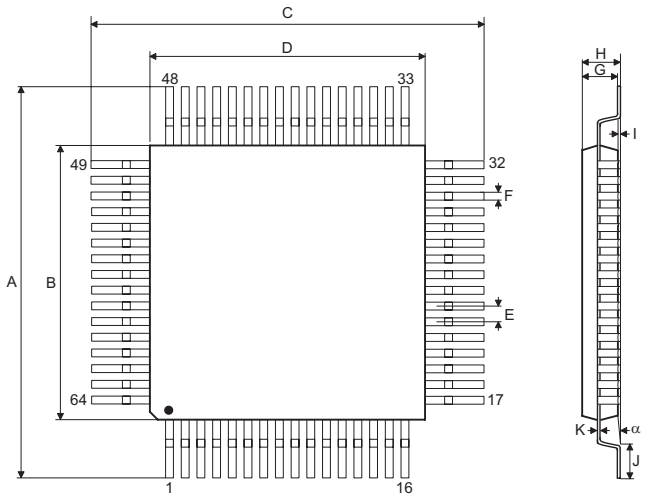
48-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°