

**PATENTED**  
**PAT No. : 099352**

### Features

- Operating voltage: 2.7V~5.2V
- External Crystal 32.768kHz oscillator
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 32×8 patterns, 8 commons, 32 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base or WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selectable buzzer frequencies (2kHz or 4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- HT16220: 64pin LQFP package  
 HT16220G: Gold bumped chip

### General Description

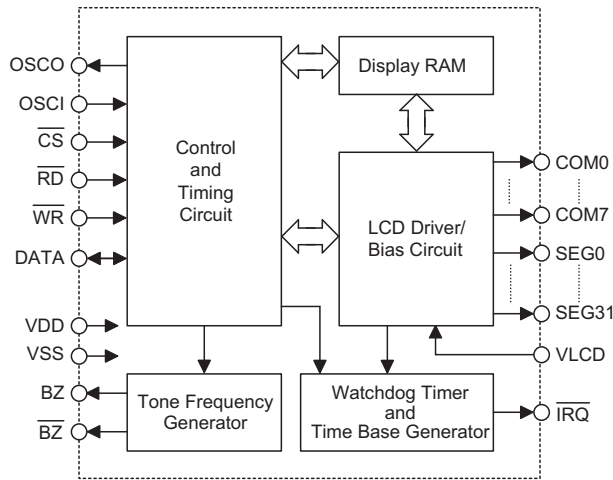
HT16220 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 256 patterns (32×8). It also supports serial interface, buzzer sound, watchdog timer or time base timer functions. The HT16220 is a memory mapping and multi-function LCD controller. The software configuration feature of the

HT16220 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the HT16220. The HT162X series have many kinds of products that match various applications.

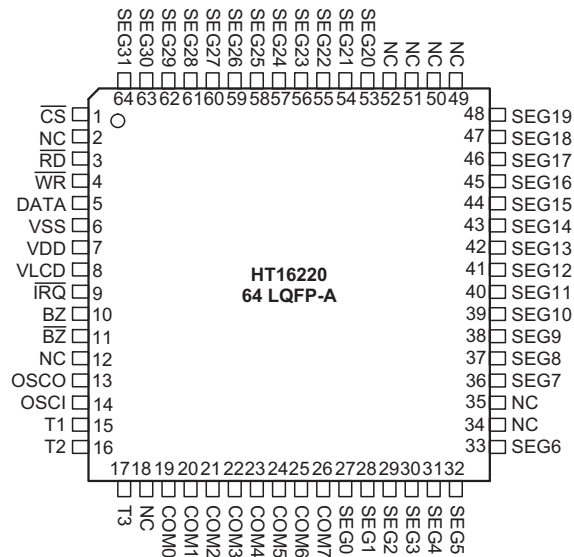
### Selection Table

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626
<b>COM</b>	4	4	8	<b>8</b>	8	8	16
<b>SEG</b>	32	32	32	<b>32</b>	48	64	48
<b>Built-in Osc.</b>	—	√	√	—	√	√	√
<b>Crystal Osc.</b>	√	√	—	√	√	√	√

Block Diagram



Pin Assignment





**Pad Coordinates**

Unit:  $\mu\text{m}$

Pad No.	X	Y	Pad No.	X	Y
1	-1068.102	1142.255	29	973.176	-1144.760
2	-1068.102	941.875	30	1072.194	-1144.760
3	-1068.102	842.776	31	1094.145	-130.495
4	-1068.102	614.987	32	1094.145	-31.395
5	-1046.545	379.670	33	1094.145	67.624
6	-1068.102	274.635	34	1094.145	166.725
7	-1068.102	175.574	35	1094.145	265.745
8	-1068.102	-1.490	36	1094.145	364.846
9	-1068.102	-213.816	37	1094.145	463.865
10	-1068.102	-403.664	38	1094.145	562.966
11	-1068.102	-608.980	39	1094.145	661.984
12	-1068.102	-708.000	40	1094.145	761.086
13	-1068.102	-858.985	41	1094.145	860.104
14	-1068.102	-958.005	42	1094.145	959.206
15	-1068.102	-1124.635	43	1094.145	1058.224
16	-546.419	-1144.760	44	233.365	1142.380
17	-447.320	-1144.760	45	134.264	1142.380
18	-255.590	-1144.760	46	35.245	1142.380
19	-156.490	-1144.760	47	-63.855	1142.380
20	35.241	-1144.760	48	-162.874	1142.380
21	134.340	-1144.760	49	-261.975	1142.380
22	279.715	-1144.760	50	-360.995	1142.380
23	378.815	-1144.760	51	-460.096	1142.380
24	477.835	-1144.760	52	-559.115	1142.380
25	576.935	-1144.760	53	-658.216	1142.380
26	675.954	-1144.760	54	-757.234	1142.380
27	775.056	-1144.760	55	-856.334	1142.380
28	874.074	-1144.760			

**Pad Description**

Pad No.	Pad Name	I/O	Description
1	$\overline{CS}$	I	Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or written to the HT16220 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT16220 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor. Data in the RAM of the HT16220 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT16220 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input or output with pull-high resistor
5	VSS	—	Negative power supply, ground
6	VDD	—	Positive power supply
7	VLCD	I	LCD operating voltage input pad.
8	$\overline{IRQ}$	O	Time base or watchdog timer overflow flag, NMOS open drain output.
9, 10	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
11	OSCO	O	Crystal oscillator output pin
12	OSCI	I	Crystal oscillator input pin
13~15	T1~T3	I	Not connected
16~23	COM0~COM7	O	LCD common outputs
24~55	SEG0~SEG31	O	LCD segment outputs

**Absolute Maximum Ratings**

Supply Voltage .....-0.3V to 5.5V      Storage Temperature .....-50°C to 125°C  
 Input Voltage ..... $V_{SS}-0.3V$  to  $V_{DD}+0.3V$       Operating Temperature .....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>DD</sub>	Operating Voltage	—	—	2.7	—	5.2	V
I <sub>DD1</sub>	Operating Current	3V	No load or LCD ON	—	—	50	μA
		5V	Crystal oscillator	—	—	65	μA
I <sub>DD2</sub>	Operating Current	3V	No load or LCD OFF	—	—	20	μA
		5V	Crystal oscillator	—	—	30	μA
I <sub>STB</sub>	Standby Current	3V	No load, Power down mode	—	1	8	μA
		5V		—	2	16	μA
V <sub>IL</sub>	Input Low Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>IH</sub>	Input High Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I <sub>OL1</sub>	BZ, $\overline{BZ}$ , $\overline{IRQ}$	3V	V <sub>OL</sub> =0.3V	0.9	1.8	—	mA
		5V	V <sub>OL</sub> =0.5V	1.7	3.0	—	mA
I <sub>OH1</sub>	BZ, $\overline{BZ}$	3V	V <sub>OH</sub> =2.7V	-0.9	-1.8	—	mA
		5V	V <sub>OH</sub> =4.5V	-1.7	-3.0	—	mA
I <sub>OL1</sub>	DATA	3V	V <sub>OL</sub> =0.3V	200	450	—	μA
		5V	V <sub>OL</sub> =0.5V	250	500	—	μA
I <sub>OH1</sub>	DATA	3V	V <sub>OH</sub> =2.7V	-200	-450	—	μA
		5V	V <sub>OH</sub> =4.5V	-250	-500	—	μA
I <sub>OL2</sub>	LCD Common Sink Current	3V	V <sub>OL</sub> =0.3V	15	40	—	μA
		5V	V <sub>OL</sub> =0.5V	100	200	—	μA
I <sub>OH2</sub>	LCD Common Source Current	3V	V <sub>OH</sub> =2.7V	-15	-30	—	μA
		5V	V <sub>OH</sub> =4.5V	-45	-90	—	μA
I <sub>OL3</sub>	LCD Segment Sink Current	3V	V <sub>OL</sub> =0.3V	15	30	—	μA
		5V	V <sub>OL</sub> =0.5V	70	150	—	μA
I <sub>OH3</sub>	LCD Segment Source Current	3V	V <sub>OH</sub> =2.7V	-6	-13	—	μA
		5V	V <sub>OH</sub> =4.5V	-20	-40	—	μA
R <sub>PH</sub>	Pull-high Resistor	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	100	200	300	kΩ
		5V		50	100	150	kΩ

**A.C. Characteristics**

T<sub>a</sub>=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
f <sub>SYS</sub>	System Clock	—	Crystal oscillator	—	32768	—	Hz
		—	External clock source	—	32768	—	Hz
f <sub>LCD</sub>	LCD Frame Frequency	—	Crystal oscillator	—	64	—	Hz
t <sub>COM</sub>	LCD Common Period	—	n: Number of COM	—	n/f <sub>LCD</sub>	—	sec
f <sub>CLK1</sub>	Serial Data Clock ( $\overline{WR}$ Pin)	3V	Duty cycle 50%	4	—	150	kHz
		5V		4	—	300	kHz
f <sub>CLK2</sub>	Serial Data Clock ( $\overline{RD}$ Pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
t <sub>CS</sub>	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	500	600	—	ns
t <sub>CLK</sub>	$\overline{WR}$ , $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	125	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	125	μs
			Read mode	3.34	—	—	

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
t <sub>r</sub> , t <sub>f</sub>	Rise/Fall Time Serial Data Clock (Figure 1)	—	—	—	120	160	ns
t <sub>SU</sub>	Setup Time for DATA to $\overline{WR}$ , $\overline{RD}$ Serial Data Clock (Figure 2)	—	—	60	120	—	ns
t <sub>h</sub>	Hold Time for DATA to $\overline{WR}$ , $\overline{RD}$ Serial Data Clock (Figure 2)	—	—	500	600	—	ns
t <sub>SU1</sub>	Setup Time for $\overline{CS}$ to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 3)	—	—	500	600	—	ns
t <sub>h1</sub>	Hold Time for $\overline{CS}$ to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 3)	—	—	700	800	—	ns
f <sub>tone</sub>	Tone Frequency (2kHz)	—	Crystal oscillator	—	2	—	kHz
	Tone Frequency (4kHz)	—	Crystal oscillator	—	4	—	kHz
t <sub>OFF</sub>	V <sub>DD</sub> OFF Times (Figure 4)	—	V <sub>DD</sub> drop down to 0V	20	—	—	ms
t <sub>SR</sub>	V <sub>DD</sub> Rising Slew Rate (Figure 4)	—	—	0.05	—	—	V/ms
t <sub>RSTD</sub>	Delay Time after Reset (Figure 4)	—	—	1	—	—	ms

- Note:
1. If the conditions of Power-on Reset timing are not satisfied in power On/Off sequence, the internal Power-on Reset (POR) circuit will not operate normally.
  2. If the V<sub>DD</sub> drops below the minimum voltage of operating voltage spec. during operating, the conditions of Power-on Reset timing must be satisfied also. That is, the V<sub>DD</sub> must drop to 0V and keep at 0V for 20ms (min.) before rising to the normal operating voltage.

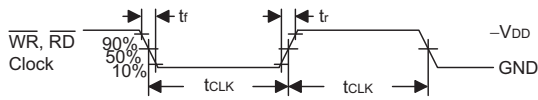


Figure 1

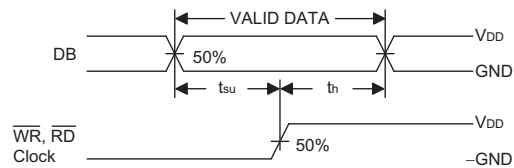


Figure 2

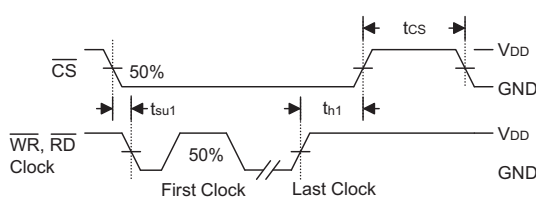


Figure 3

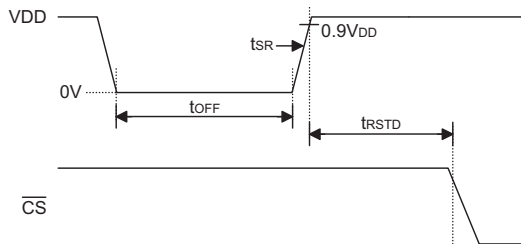


Figure 4. Power-on Reset Timing

**Functional Description**

**Display Memory – RAM Structure**

The static display RAM is organized into 64x4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

**Time Base and Watchdog Timer – WDT**

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the  $\overline{\text{IRQ}}$  pin will stay at a logic low level until the CLR WDT or the  $\overline{\text{IRQ}}$  DIS command is issued.

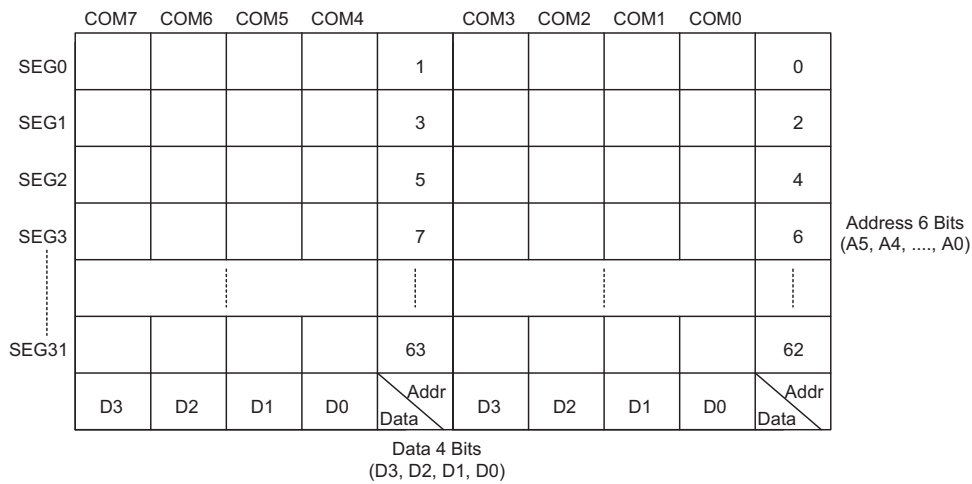
If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

**Buzzer Tone Output**

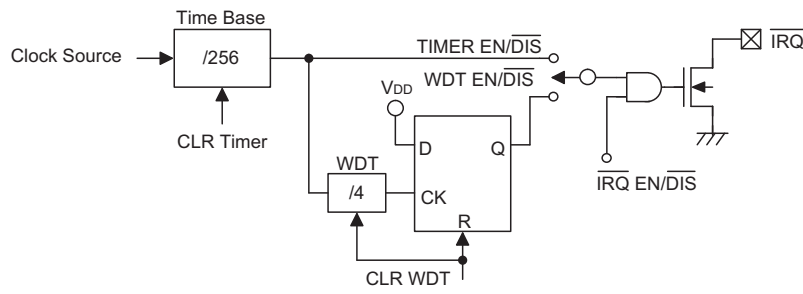
A simple tone generator is implemented in the HT16220. The tone generator can output a pair of differential driving signals on the BZ and  $\overline{\text{BZ}}$  which are used to generate a single tone.

**Command Format**

The HT16220 can be configured by the software setting. There are two mode commands to configure the HT16220 resource and to transfer the LCD display data.



**RAM Mapping**



**Timer and WDT Configurations**



The following are the data mode ID and the command mode ID:

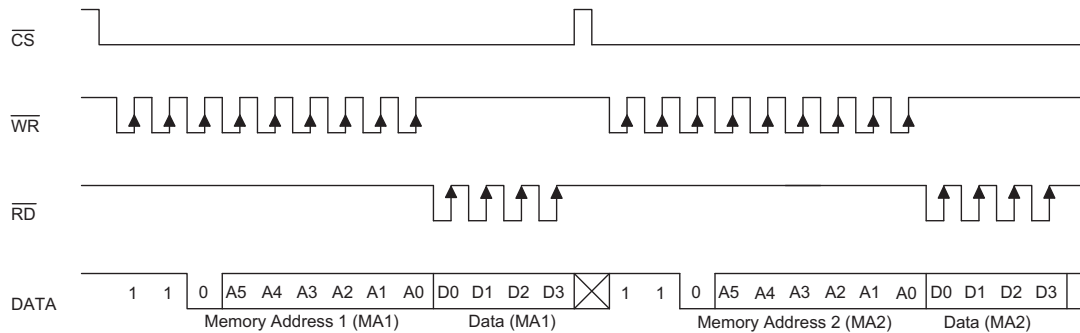
Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the  $\overline{CS}$  pin should be set to "1" and the previous operation mode will be reset also. The  $\overline{CS}$  pin returns to "0", a new operation mode ID should be issued first.

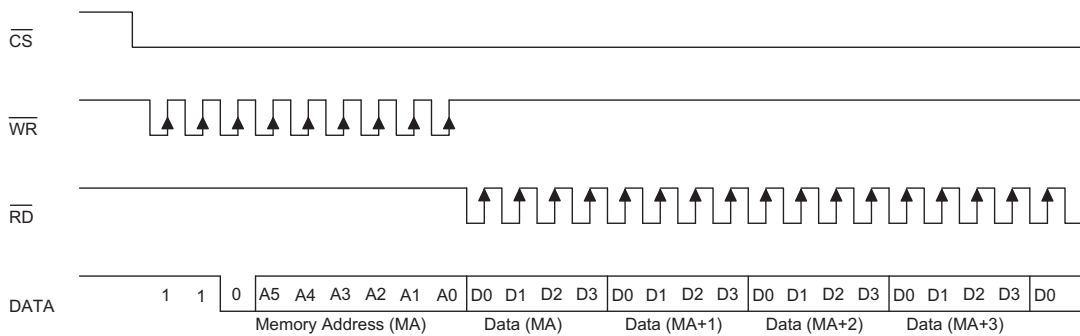
Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

### Timing Diagrams

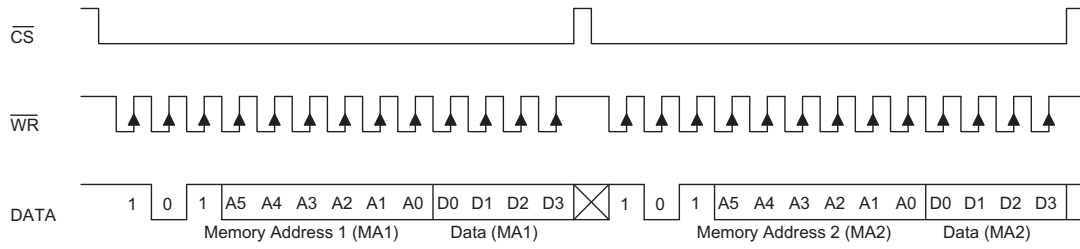
#### READ Mode (Command Code : 1 1 0)



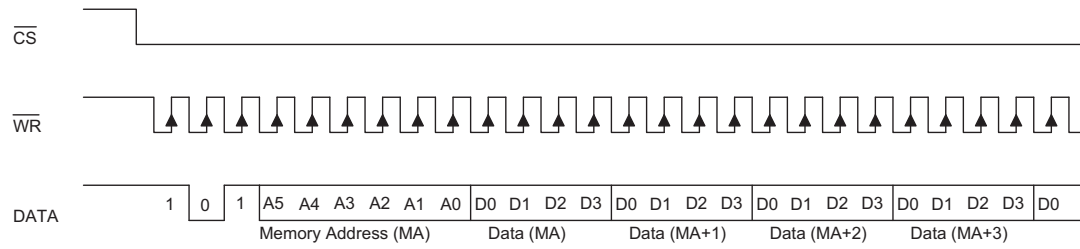
#### READ mode (successive address reading)



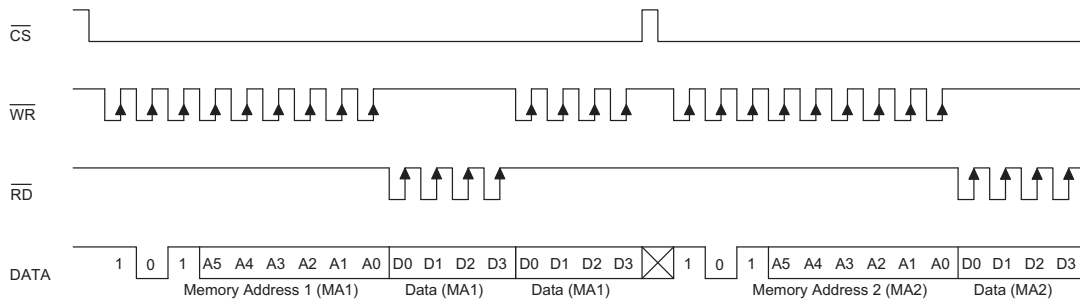
**WRITE Mode (Command Code : 1 0 1)**



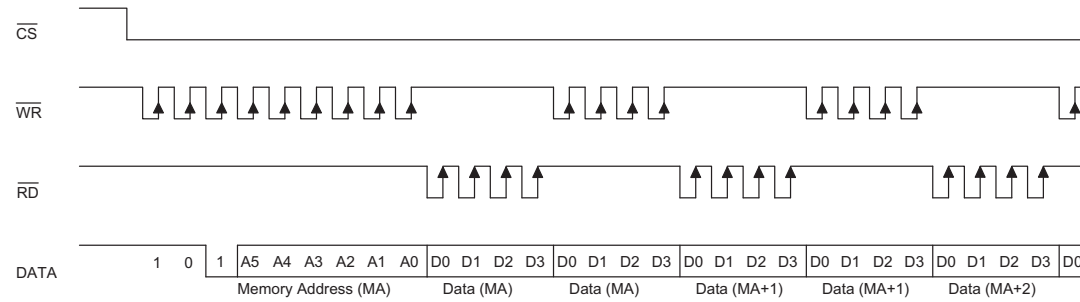
**WRITE Mode (Successive Address Writing)**



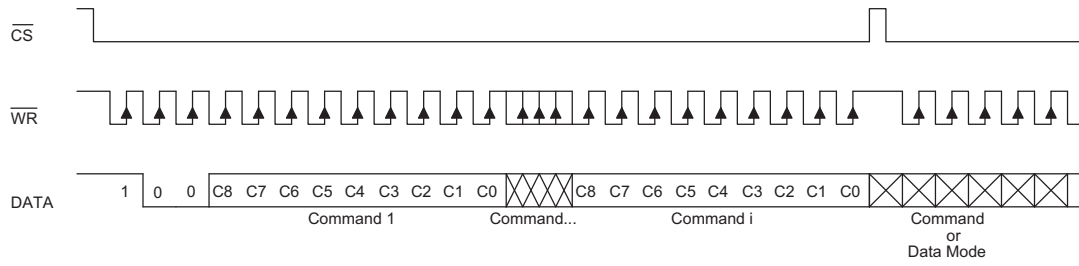
**READ-MODIFY-WRITE Mode (Command Code : 1 0 1)**



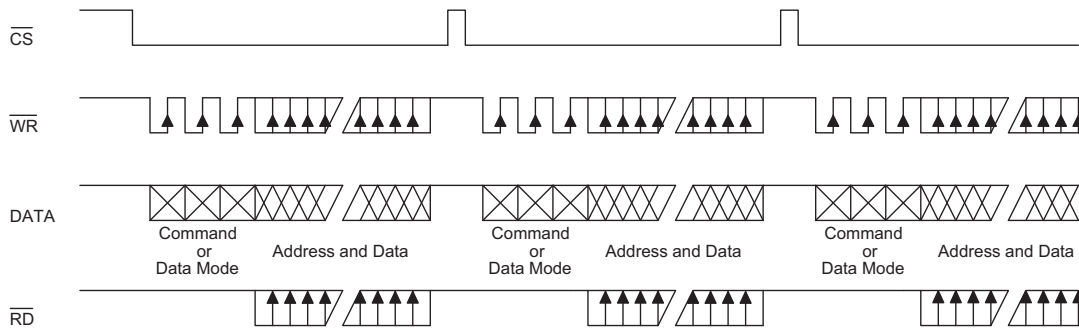
**READ-MODIFY-WRITE Mode (Successive Address Accessing)**



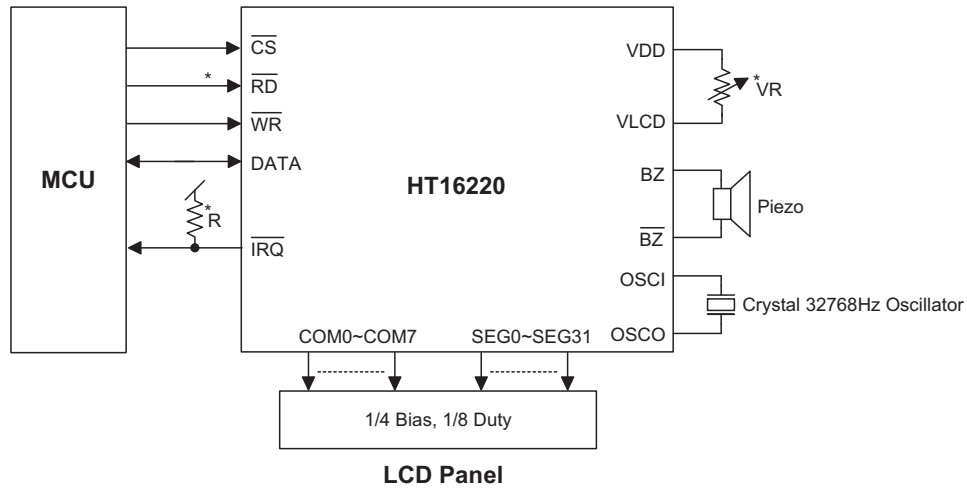
**Command Mode (Command Code : 1 0 0)**



**Mode (Data And Command Mode)**



Application Circuits



Note: The connection of  $\overline{\text{IRQ}}$  and  $\overline{\text{RD}}$  pin can be selected depending on the requirement of the MCU.  
 The voltage applied to  $V_{\text{LCD}}$  pin must be equal to or lower than  $V_{\text{DD}}$ .  
 Adjust VR to fit user's LCD panel display voltage ( $V_{\text{LCD}}$ ).  
 Adjust R (external pull-high resistance) to fit user's time base clock.

Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD display	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD display	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	Yes
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	Yes
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
CLR TIMER	1 0 0	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	1 0 0	0000-1111-X	C	Clear the contents of the WDT stage	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	1 0 0	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{\text{IRQ}}$ DIS	1 0 0	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	1 0 0	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	

Name	ID	Command Code	D/C	Function	Def.
F1	<b>1 0 0</b>	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	<b>1 0 0</b>	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	<b>1 0 0</b>	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	<b>1 0 0</b>	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	<b>1 0 0</b>	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	
F32	<b>1 0 0</b>	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	<b>1 0 0</b>	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	<b>1 0 0</b>	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	Yes
TEST	<b>1 0 0</b>	1110-0000-X	C	Test mode, user don't use.	
NORMAL	<b>1 0 0</b>	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

A5~A0 : RAM address

D3~D0 : RAM data

D/C : Data/Command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from a 32.768kHz crystal oscillator or an external 32768Hz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT16220 after power on reset, for power on reset may fail, which in turn leads to malfunctioning of the HT16220.

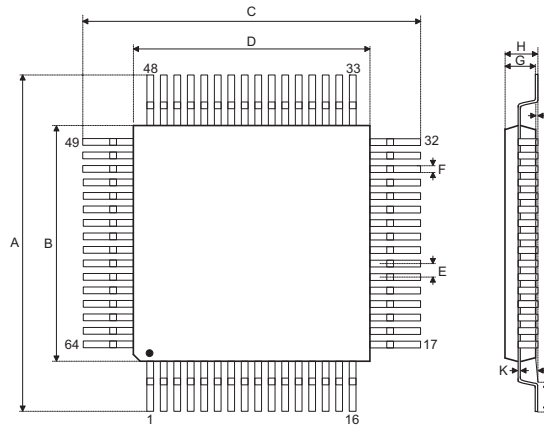
**Package Information**

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Further Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [Packing Materials Information](#)
- [Carton information](#)

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
$\alpha$	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
$\alpha$	0°	—	7°

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