Feature

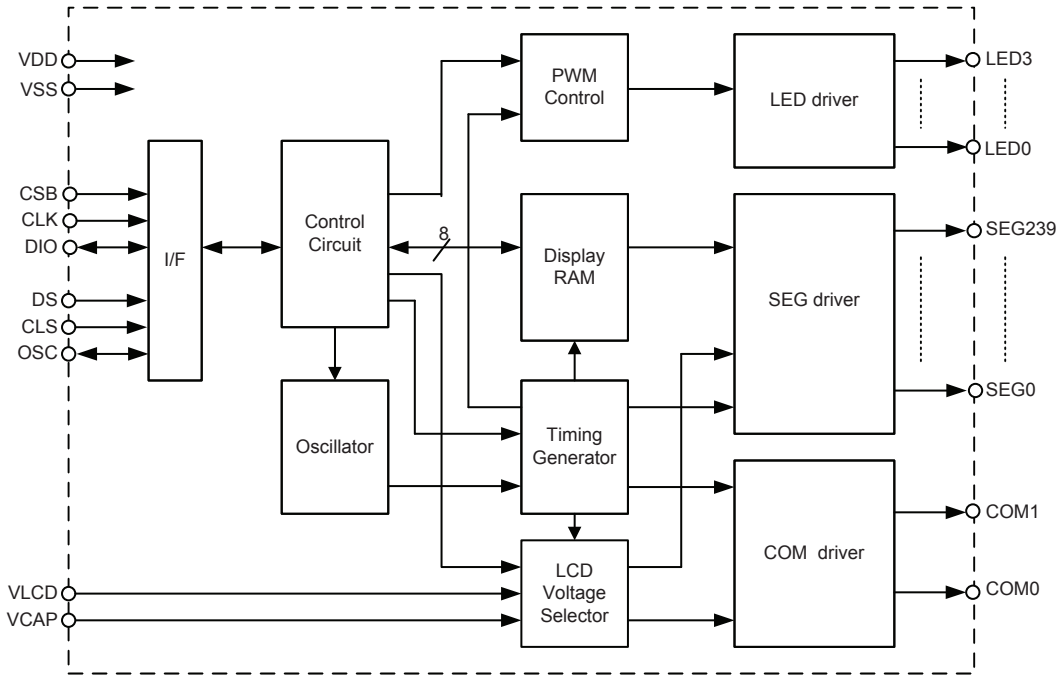
- Logic operating voltage: 2.4V~5.5V
- LCD operating voltage: 2.4V~5.5V
- LCD display: Max. 240 Segments and 2 Commons
- LCD display data RAM: 60×8 bits=480 bits
- Duty: static, 1/2; Bias: 1/1, 1/2
- External VLCD pin to supply LCD operating voltage
- Internal 51.2kHz RC oscillator
- 4-Chanel LED driver
  - Supports up to 16 level PWM luminance control
- SPI 3-wire serial interface
- Package type: COG – 60μm min.

General Description

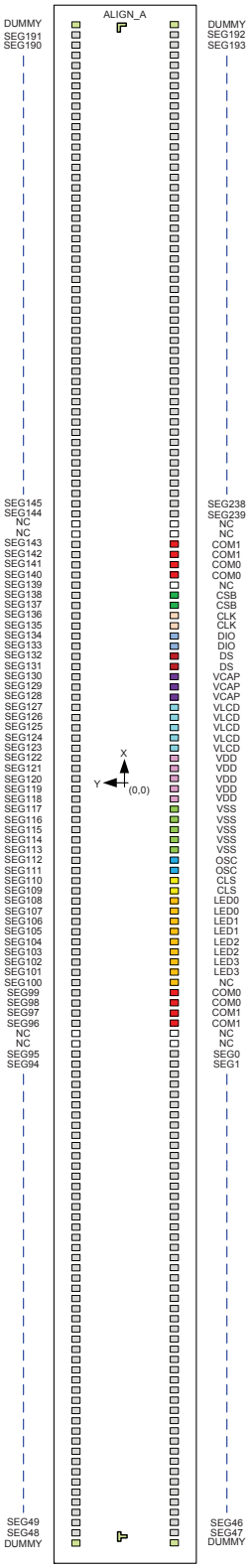
The HT1629G is a memory mapping and multi-function LCD controller driver which can be switched to either 1/1 or 1/2 duty. It can display up to 240 patterns with a 1/1 duty or 480 patterns with a 1/2 duty driver output. It supports a common driver output mode segment / LED driver. The software configuration features of the device makes it suitable for multiple LCD applications including LCD modules and display subsystems.

The HT1629G is compatible with most micro-controllers and communicates via a three-line SPI interface.

Block Diagram



COG Pad Assignment

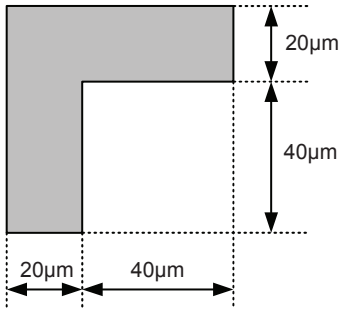
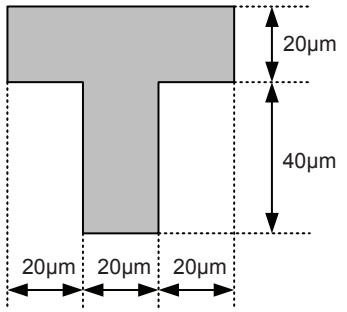


Note: The IC substrate should be connected to V_{SS} in the PCB layout artwork.

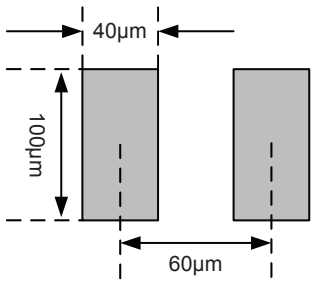
COG Chip Dimensions

Item	Number		Size		Unit
			X	Y	
Chip size	—		9132	794	μm
Chip thickness	—		508±20		μm
Bump spacing	—		20		μm
Bump pitch	—		60		μm
Bump size	Output pad	—	40	100	μm
	Input pad	—	40	100	μm
	Dummy pad	—	40	100	μm
	NC pad	—	40	100	μm
Bump height	All pad		18±3		μm

COG Alignment mark Dimensions

Item	Number	Size	Unit
ALIGN_A	302		μm
ALIGN_B	151		μm

COG Pad Dimensions

Item	Number	Size	Unit
Output pad	—		μm
Input pad			
Dummy pad			

COG Pad Coordinates

Unit: μm

No	Name	X	Y	No	Name	X	Y
1	Dummy	4470.000	287.500	152	DUMMY	-4470.000	-287.500
2	SEG191	4410.000	287.500	153	SEG47	-4410.000	-287.500
3	SEG190	4350.000	287.500	154	SEG46	-4350.000	-287.500
4	SEG189	4290.000	287.500	155	SEG45	-4290.000	-287.500
5	SEG188	4230.000	287.500	156	SEG44	-4230.000	-287.500
6	SEG187	4170.000	287.500	157	SEG43	-4170.000	-287.500
7	SEG186	4110.000	287.500	158	SEG42	-4110.000	-287.500
8	SEG185	4050.000	287.500	159	SEG41	-4050.000	-287.500
9	SEG184	3990.000	287.500	160	SEG40	-3990.000	-287.500
10	SEG183	3930.000	287.500	161	SEG39	-3930.000	-287.500
11	SEG182	3870.000	287.500	162	SEG38	-3870.000	-287.500
12	SEG181	3810.000	287.500	163	SEG37	-3810.000	-287.500
13	SEG180	3750.000	287.500	164	SEG36	-3750.000	-287.500
14	SEG179	3690.000	287.500	165	SEG35	-3690.000	-287.500
15	SEG178	3630.000	287.500	166	SEG34	-3630.000	-287.500
16	SEG177	3570.000	287.500	167	SEG33	-3570.000	-287.500
17	SEG176	3510.000	287.500	168	SEG32	-3510.000	-287.500
18	SEG175	3450.000	287.500	169	SEG31	-3450.000	-287.500
19	SEG174	3390.000	287.500	170	SEG30	-3390.000	-287.500
20	SEG173	3330.000	287.500	171	SEG29	-3330.000	-287.500
21	SEG172	3270.000	287.500	172	SEG28	-3270.000	-287.500
22	SEG171	3210.000	287.500	173	SEG27	-3210.000	-287.500
23	SEG170	3150.000	287.500	174	SEG26	-3150.000	-287.500
24	SEG169	3090.000	287.500	175	SEG25	-3090.000	-287.500
25	SEG168	3030.000	287.500	176	SEG24	-3030.000	-287.500
26	SEG167	2970.000	287.500	177	SEG23	-2970.000	-287.500
27	SEG166	2910.000	287.500	178	SEG22	-2910.000	-287.500
28	SEG165	2850.000	287.500	179	SEG21	-2850.000	-287.500
29	SEG164	2790.000	287.500	180	SEG20	-2790.000	-287.500
30	SEG163	2730.000	287.500	181	SEG19	-2730.000	-287.500
31	SEG162	2670.000	287.500	182	SEG18	-2670.000	-287.500
32	SEG161	2610.000	287.500	183	SEG17	-2610.000	-287.500
33	SEG160	2550.000	287.500	184	SEG16	-2550.000	-287.500
34	SEG159	2490.000	287.500	185	SEG15	-2490.000	-287.500
35	SEG158	2430.000	287.500	186	SEG14	-2430.000	-287.500
36	SEG157	2370.000	287.500	187	SEG13	-2370.000	-287.500
37	SEG156	2310.000	287.500	188	SEG12	-2310.000	-287.500
38	SEG155	2250.000	287.500	189	SEG11	-2250.000	-287.500
39	SEG154	2190.000	287.500	190	SEG10	-2190.000	-287.500
40	SEG153	2130.000	287.500	191	SEG9	-2130.000	-287.500
41	SEG152	2070.000	287.500	192	SEG8	-2070.000	-287.500
42	SEG151	2010.000	287.500	193	SEG7	-2010.000	-287.500
43	SEG150	1950.000	287.500	194	SEG6	-1950.000	-287.500
44	SEG149	1890.000	287.500	195	SEG5	-1890.000	-287.500
45	SEG148	1830.000	287.500	196	SEG4	-1830.000	-287.500
46	SEG147	1770.000	287.500	197	SEG3	-1770.000	-287.500

No	Name	X	Y	No	Name	X	Y
47	SEG146	1710.000	287.500	198	SEG2	-1710.000	-287.500
48	SEG145	1650.000	287.500	199	SEG1	-1650.000	-287.500
49	SEG144	1590.000	287.500	200	SEG0	-1590.000	-287.500
50	NC	1530.000	287.500	201	NC	-1530.000	-287.500
51	NC	1470.000	287.500	202	NC	-1470.000	-287.500
52	SEG143	1410.000	287.500	203	COM1	-1410.000	-287.500
53	SEG142	1350.000	287.500	204	COM1	-1350.000	-287.500
54	SEG141	1290.000	287.500	205	COM0	-1290.000	-287.500
55	SEG140	1230.000	287.500	206	COM0	-1230.000	-287.500
56	SEG139	1170.000	287.500	207	NC	-1170.000	-287.500
57	SEG138	1110.000	287.500	208	LED3	-1110.000	-287.500
58	SEG137	1050.000	287.500	209	LED3	-1050.000	-287.500
59	SEG136	990.000	287.500	210	LED2	-990.000	-287.500
60	SEG135	930.000	287.500	211	LED2	-930.000	-287.500
61	SEG134	870.000	287.500	212	LED1	-870.000	-287.500
62	SEG133	810.000	287.500	213	LED1	-810.000	-287.500
63	SEG132	750.000	287.500	214	LED0	-750.000	-287.500
64	SEG131	690.000	287.500	215	LED0	-690.000	-287.500
65	SEG130	630.000	287.500	216	CLS	-630.000	-287.500
66	SEG129	570.000	287.500	217	CLS	-570.000	-287.500
67	SEG128	510.000	287.500	218	OSC	-510.000	-287.500
68	SEG127	450.000	287.500	219	OSC	-450.000	-287.500
69	SEG126	390.000	287.500	220	VSS	-390.000	-287.500
70	SEG125	330.000	287.500	221	VSS	-330.000	-287.500
71	SEG124	270.000	287.500	222	VSS	-270.000	-287.500
72	SEG123	210.000	287.500	223	VSS	-210.000	-287.500
73	SEG122	150.000	287.500	224	VSS	-150.000	-287.500
74	SEG121	90.000	287.500	225	VDD	-90.000	-287.500
75	SEG120	30.000	287.500	226	VDD	-30.000	-287.500
76	SEG119	-30.000	287.500	227	VDD	30.000	-287.500
77	SEG118	-90.000	287.500	228	VDD	90.000	-287.500
78	SEG117	-150.000	287.500	229	VDD	150.000	-287.500
79	SEG116	-210.000	287.500	230	VLCD	210.000	-287.500
80	SEG115	-270.000	287.500	231	VLCD	270.000	-287.500
81	SEG114	-330.000	287.500	232	VLCD	330.000	-287.500
82	SEG113	-390.000	287.500	233	VLCD	390.000	-287.500
83	SEG112	-450.000	287.500	234	VLCD	450.000	-287.500
84	SEG111	-510.000	287.500	235	VCAP	510.000	-287.500
85	SEG110	-570.000	287.500	236	VCAP	570.000	-287.500
86	SEG109	-630.000	287.500	237	VCAP	630.000	-287.500
87	SEG108	-690.000	287.500	238	DS	690.000	-287.500
88	SEG107	-750.000	287.500	239	DS	750.000	-287.500
89	SEG106	-810.000	287.500	240	DIO	810.000	-287.500
90	SEG105	-870.000	287.500	241	DIO	870.000	-287.500
91	SEG104	-930.000	287.500	242	CLK	930.000	-287.500
92	SEG103	-990.000	287.500	243	CLK	990.000	-287.500
93	SEG102	-1050.000	287.500	244	CSB	1050.000	-287.500
94	SEG101	-1110.000	287.500	245	CSB	1110.000	-287.500

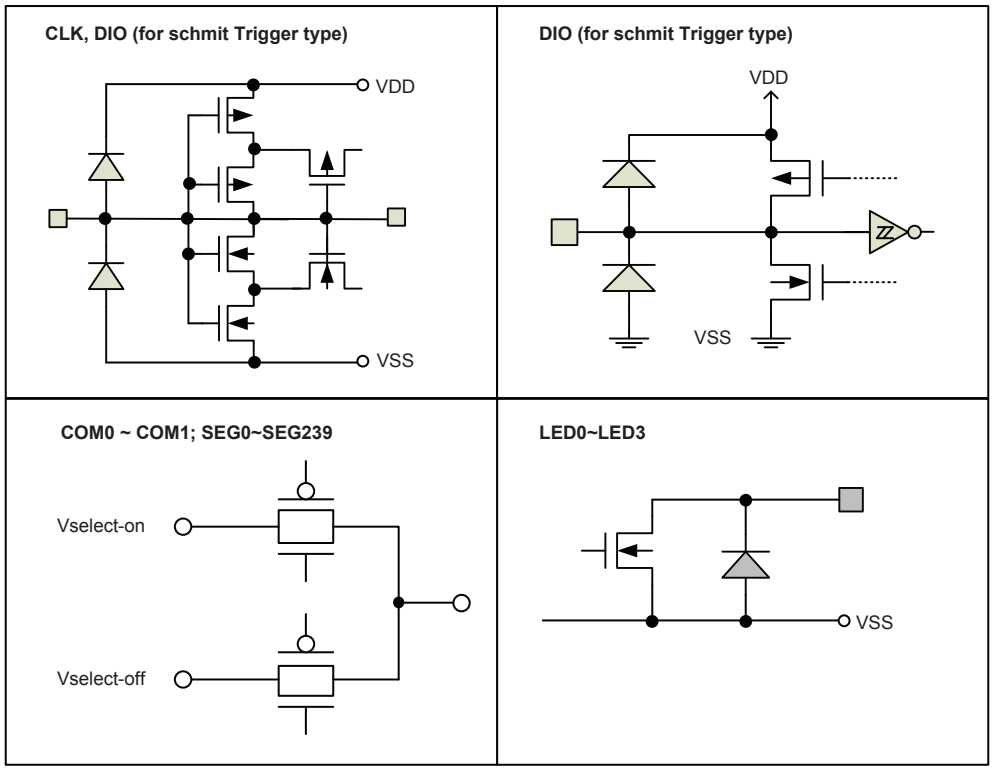
No	Name	X	Y	No	Name	X	Y
95	SEG100	-1170.000	287.500	246	NC	1170.130	-287.500
96	SEG99	-1230.000	287.500	247	COM0	1230.000	-287.500
97	SEG98	-1290.000	287.500	248	COM0	1290.000	-287.500
98	SEG97	-1350.000	287.500	249	COM1	1350.000	-287.500
99	SEG96	-1410.000	287.500	250	COM1	1410.000	-287.500
100	NC	-1470.000	287.500	251	NC	1470.000	-287.500
101	NC	-1530.000	287.500	252	NC	1530.000	-287.500
102	SEG95	-1590.000	287.500	253	SEG239	1590.000	-287.500
103	SEG94	-1650.000	287.500	254	SEG238	1650.000	-287.500
104	SEG93	-1710.000	287.500	255	SEG237	1710.000	-287.500
105	SEG92	-1770.000	287.500	256	SEG236	1770.000	-287.500
106	SEG91	-1830.000	287.500	257	SEG235	1830.000	-287.500
107	SEG90	-1890.000	287.500	258	SEG234	1890.000	-287.500
108	SEG89	-1950.000	287.500	259	SEG233	1950.000	-287.500
109	SEG88	-2010.000	287.500	260	SEG232	2010.000	-287.500
110	SEG87	-2070.000	287.500	261	SEG231	2070.000	-287.500
111	SEG86	-2130.000	287.500	262	SEG230	2130.000	-287.500
112	SEG85	-2190.000	287.500	263	SEG229	2190.000	-287.500
113	SEG84	-2250.000	287.500	264	SEG228	2250.000	-287.500
114	SEG83	-2310.000	287.500	265	SEG227	2310.000	-287.500
115	SEG82	-2370.000	287.500	266	SEG226	2370.000	-287.500
116	SEG81	-2430.000	287.500	267	SEG225	2430.000	-287.500
117	SEG80	-2490.000	287.500	268	SEG224	2490.000	-287.500
118	SEG79	-2550.000	287.500	269	SEG223	2550.000	-287.500
119	SEG78	-2610.000	287.500	270	SEG222	2610.000	-287.500
120	SEG77	-2670.000	287.500	271	SEG221	2670.000	-287.500
121	SEG76	-2730.000	287.500	272	SEG220	2730.000	-287.500
122	SEG75	-2790.000	287.500	273	SEG219	2790.000	-287.500
123	SEG74	-2850.000	287.500	274	SEG218	2850.000	-287.500
124	SEG73	-2910.000	287.500	275	SEG217	2910.000	-287.500
125	SEG72	-2970.000	287.500	276	SEG216	2970.000	-287.500
126	SEG71	-3030.000	287.500	277	SEG215	3030.000	-287.500
127	SEG70	-3090.000	287.500	278	SEG214	3090.000	-287.500
128	SEG69	-3150.000	287.500	279	SEG213	3150.000	-287.500
129	SEG68	-3210.000	287.500	280	SEG212	3210.000	-287.500
130	SEG67	-3270.000	287.500	281	SEG211	3270.000	-287.500
131	SEG66	-3330.000	287.500	282	SEG210	3330.000	-287.500
132	SEG65	-3390.000	287.500	283	SEG209	3390.000	-287.500
133	SEG64	-3450.000	287.500	284	SEG208	3450.000	-287.500
134	SEG63	-3510.000	287.500	285	SEG207	3510.000	-287.500
135	SEG62	-3570.000	287.500	286	SEG206	3570.000	-287.500
136	SEG61	-3630.000	287.500	287	SEG205	3630.000	-287.500
137	SEG60	-3690.000	287.500	288	SEG204	3690.000	-287.500
138	SEG59	-3750.000	287.500	289	SEG203	3750.000	-287.500
139	SEG58	-3810.000	287.500	290	SEG202	3810.000	-287.500
140	SEG57	-3870.000	287.500	291	SEG201	3870.000	-287.500
141	SEG56	-3930.000	287.500	292	SEG200	3930.000	-287.500
142	SEG55	-3990.000	287.500	293	SEG199	3990.000	-287.500

No	Name	X	Y	No	Name	X	Y
143	SEG54	-4050.000	287.500	294	SEG198	4050.000	-287.500
144	SEG53	-4110.000	287.500	295	SEG197	4110.000	-287.500
145	SEG52	-4170.000	287.500	296	SEG196	4170.000	-287.500
146	SEG51	-4230.000	287.500	297	SEG195	4230.000	-287.500
147	SEG50	-4290.000	287.500	298	SEG194	4290.000	-287.500
148	SEG49	-4350.000	287.500	299	SEG193	4350.000	-287.500
149	SEG48	-4410.000	287.500	300	SEG192	4410.000	-287.500
150	DUMMY	-4470.000	287.500	301	DUMMY	4470.000	-287.500
151	ALIGN_B	-4429.000	20.000	302	ALIGN_A	4449.000	20.000

Pad Description

Pad Name	Type	Description
VDD	—	Positive power supply
VSS	—	Negative power supply, ground
VLCD	—	LCD power supply
CSB	I	Chip select input This input pin has an integrated RC filter circuit with a 50 MHz cut-off frequency
CLK	I	Serial clock input pin. This input pin has an integrated RC filter circuit with a 50 MHz cut-off frequency
DIO	I/O	Serial data input/output pin. The data is input on or comes out of the shift register at the rising edge of the clock CMOS output. This input pin has an integrated RC filter circuit with a 50 MHz cut-off frequency
VCAP	I	1/2 bias voltage input pin. A capacitor should be connected between this pin and VSS. When DS='1' a capacitor should be connected between this pin and VSS. When DS='0' this is the 1/2 duty condition and the pin is used as an LCD bias voltage input. Here a resistor divider should be connected between the VLCD pin and VSS pin or an externally supplied voltage input supplied to obtain a voltage equal to 1/2 VLCD.
DS	I	Duty select pin. DS='1': Static, COM0 and COM1 output the same waveform DS='0': 1/2 duty
CLS	I	This pin is used to enable the internal clock. When this pin is pulled high, the internal clock is enabled. If the pin is low, the internal clock will be disabled and an external clock source must be connected to the OSC pin for normal operation. This input pin has an integrated RC filter circuit with a 50 MHz cut-off frequency.
OSC	I	System clock input
COM0 ~ COM1	O	LCD Common output
SEG0 ~ SEG239	O	LCD Segment output
LED0~LED3	O	LED driver outputs pins – NMOS open-drain

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.5V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -55°C to 150°C

Operating Temperature ..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta= -40°C ~ 85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	LCD Operating Voltage	—	—	2.4	—	5.5	V
I_{STB_VDD}	Standby Current	3.3V	No load, 1/1 duty Power Down Mode	—	—	1	μA
		5V		—	—	1	μA
I_{STB_VLCD}	Standby Current	3.3V	No load, 1/1 duty Power Down Mode	—	—	1	μA
		5V		—	—	1	μA
I_{DD1}	Operating Current	3.3V	No load, SYS EN LCD On, 1/1 duty	—	10	20	μA
		5V		—	20	40	μA
I_{DD2}	Operating Current	3.3V	No load, SYS EN LCD Off, 1/1 duty	—	10	20	μA
		5V		—	20	40	μA
I_{LCD}	Operating Current	3.3V	No load, VDD=VLCD, LCD On, 1/1 duty	—	2	4	μA
		5V		—	3	6	μA
V_{IH}	Input High Voltage	3.3V	DIO, CLK, CSB	$0.7V_{DD}$	—	V_{DD}	V
		5V					V
V_{IL}	Input Low Voltage	3.3V	DI, CLK, CSB	0	—	$0.3V_{DD}$	V
		5V					V
R_{PH}	Pull-high Resistor	3.3V	CLS	40	100	170	kΩ
		5V		20	50	90	kΩ
I_{OH}	High Level Output Current	3.3V	V_{OH}=2.97V, DIO	-4.5	—	—	mA
		5V	V_{OH}=4.5V, DIO	-9.0	—	—	mA
I_{OL}	Low Level Output Current	3.3V	V_{OL}=0.33V, DIO	6	—	—	mA
		5V	V_{OL}=0.5V, DIO	12	—	—	mA
I_{OH1}	LCD Common Source Current	3.3V	V_{OH}=2.97V	-1.0	—	—	mA
		5V	V_{OH}=4.5V	-2.0	—	—	mA
I_{OL1}	LCD Common Sink Current	3.3V	V_{OL}=0.33V	2.0	—	—	mA
		5V	V_{OL}=0.5V	3.5	—	—	mA
I_{OH2}	LCD Segment Source Current	3.3V	V_{OH}=2.97V	-1.0	—	—	mA
		5V	V_{OH}=4.5V	-2.0	—	—	mA
I_{OL2}	LCD Segment Sink Current	3.3V	V_{OL}=0.33V	2.0	—	—	mA
		5V	V_{OL}=0.5V	3.3	—	—	mA
I_{OL3}	LED Sink Current	3.3V	V_{OL}=1V	10	—	—	mA
		5V	V_{OL}=2V	20	—	—	mA

A.C. Characteristics

Unless otherwise specified, V_{DD}=2.4V to 5.5V; V_{SS}=0V; Ta= -40°C~85°C

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	condition				
f_{SYS}	Oscillator Frequency	3.3	Ta=25°C,FS bit="0"	49	70	91	kHz
		5.0	Ta=25°C,FS bit="0"	39.2	56	72.8	kHz
f_{LCD}	LCD Frame Frequency	—	Ta=25°C, FS bit="0" n=1 (F_{FR}=200Hz)) or 2 (F_{FR}=100Hz)	—	f_{SYS}/ (256*n)	—	Hz
V_{POR}	V_{DD} Start voltage to ensure Power on reset	—	—	—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to ensure Power on reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to remain at V_{POR} to ensure Power on reset	—	—	10	—	—	ms

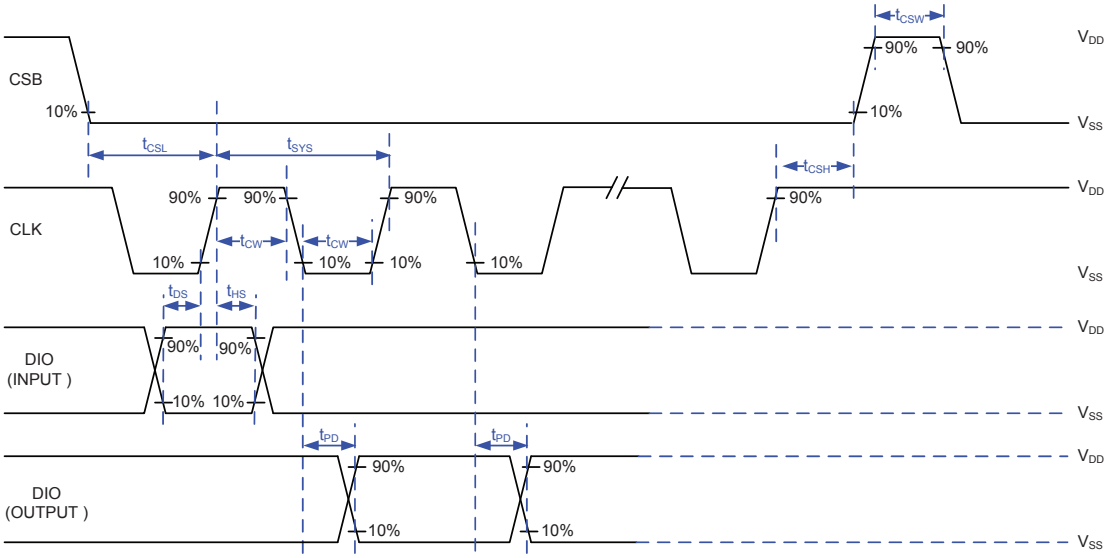
A.C. Characteristics – SPI 3-wire serial Interface

V_{DD}=2.4V to 5.5V; V_{SS}=0V; Ta= -40°C~85°C

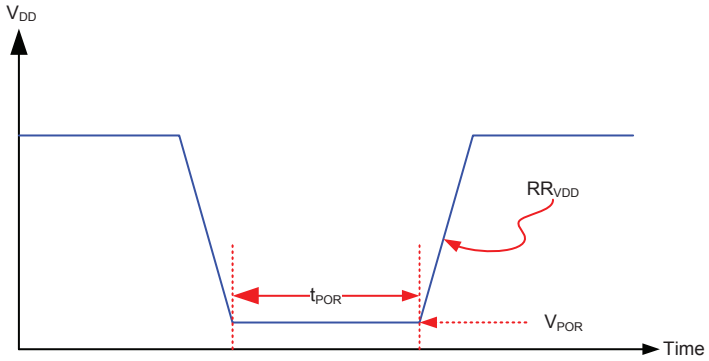
Symbol	Parameter	Test condition			Min.	Typ.	Max.	Unit
		V_{DD}	condition					
t_{SYS}	Clock cycle time	—	For write data		250	—	—	ns
t_{CW}	Clock Pulse Width	—	For write data		100	—	—	ns
t_{DS}	Data Setup Time	—	For write data		50	—	—	ns
t_{DH}	Data Hold Time	—	For write data		50	—	—	ns
t_{CSW}	"H" CSB Pulse Width	—	—		100	—	—	ns
t_{CSL}	CSB Setup Time (CSB↓ – CLK↑)	—	For write data		50	—	—	ns
t_{CSH}	CS Hold Time (CLK↑ – CSB↑)	—	—		2	—	—	µs
t_{PD}	DATA Output Delay Time (CLK – DIO)	—	C_O=15pF, Ta=25°C	t_{PD}=10 to 90%	—	—	350	ns
				t_{PD}=90 to 10%				

Timing Diagrams

SPI 3-wire serial Interface Timing



Power ON Reset Timing



Notes: 1. If the reset timing conditions are not satisfied during the power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If it is difficult to meet power on reset timing conditions, a software reset command should be executed after power on.

Functional Description

Power-on Reset

When power is applied, the devices will be initialized by the internal power-on reset circuit. The status of the internal circuit after initialization is as follows:

- All registers are set to their default value, but do not affect the RAM contests
- The System Oscillator and LCD bias generator are off
- The LCD Display is in an off state
- All common outputs are set to V_{LCD}
- All segment outputs are set to V_{LCD}
- The LEDs are in an off state
- The Frame Frequency is set to 100Hz

LCD Driver

The device is a 480 (240×2) pattern LCD driver. It can be configured with 1 or 2 commons using the DS pin configuration. This feature makes the HT1629G suitable for multiple LCD applications. The LCD clock is derived from the system clock.

DS pin	Duty	Bias
0	1/2	1/2
1	static	1/1

Note: It is not recommended to change the DS pin input value after a system enable.

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The System Clock frequency determines the LCD frame frequency. During the initial system power on the System Oscillator will be in a stop state.

LCD Bias Generator

The full-scale LCD voltage (Vop) is obtained from $V_{LCD} - V_{SS}$.

The LCD voltage may be temperature compensated externally through the Voltage supply to the V_{LCD} pin. The LCD biasing voltage is obtained from an external voltage divider composed of two series resistors connected between V_{LCD} and V_{SS}. The center resistor can be switched out of the circuit to provide a 1/1bias voltage level configuration or a 1/2bias voltage level configuration.

Segment Driver Outputs

The LCD driver section includes segment outputs which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed column signals and with the data resident in the display latch. Any unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes column outputs which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit.

Address Pointer

The addressing mechanism for the display RAM is realized using the address pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Address pointer command.

Frame Frequency

The device provides two kinds of frame frequency options using a system set command code, these are 100Hz and 200Hz.

Display Memory – RAM Structure

The display RAM is a static 60×8 bits RAM which stores the LCD data. A logic "1" in the RAM bit-map indicates an "on" state of the corresponding LCD segment while a logic 0 indicates an "off" state.

There is a one-to-one correspondence between the RAM addresses and the segment outputs and between the individual bits of a RAM word and the column outputs. The following shows the RAM to LCD pattern mapping sequence.

1. When DS='1', static. The COM1 output waveform is equal to the COM0 output waveform.

COM output								Address
COM0	COM0	COM0	COM0	COM0	COM0	COM0	COM0	
SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	00H
SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	01H
SEG16	SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	02H
SEG24	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	03H
↓	↓	↓	↓	↓	↓	↓	↓	↓
SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	1Ch
SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239	1Dh
D7	D6	D5	D4	D3	D2	D1	D0	Data byte

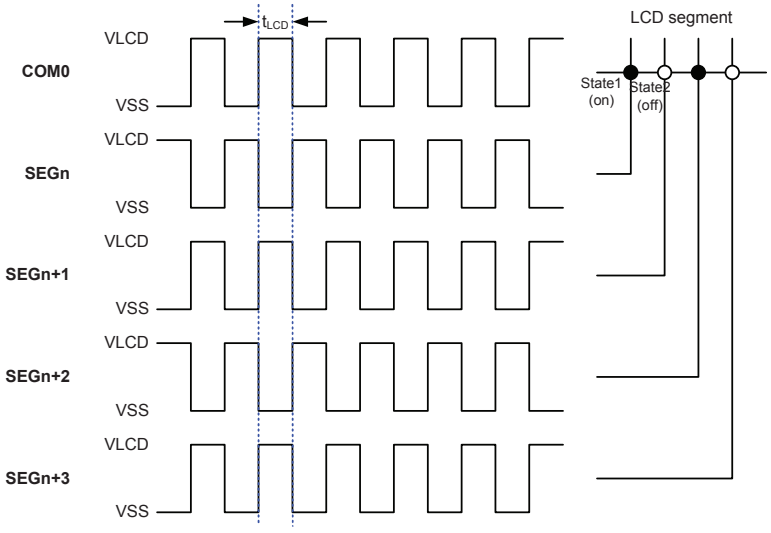
2.When DS='0', 1/2 duty

COM output								Address
COM0	COM1	COM0	COM1	COM0	COM1	COM0	COM1	
SEG0		SEG1		SEG2		SEG3		00H
SEG4		SEG5		SEG6		SEG7		01H
SEG8		SEG9		SEG10		SEG11		02H
SEG12		SEG13		SEG14		SEG15		03H
↓		↓		↓		↓		↓
SEG232		SEG233		SEG234		SEG235		3AH
SEG236		SEG237		SEG238		SEG239		3BH
D7	D6	D5	D4	D3	D2	D1	D0	Data byte

Note: It is recommended to initialize the display RAM data by clearing all RAM data before the LCD display function is activated. If the RAM data is not initialized before enabling the LCD display function, it may result in abnormal LCD display effect after executing the LCD ON command.

LCD Drive Mode Waveforms

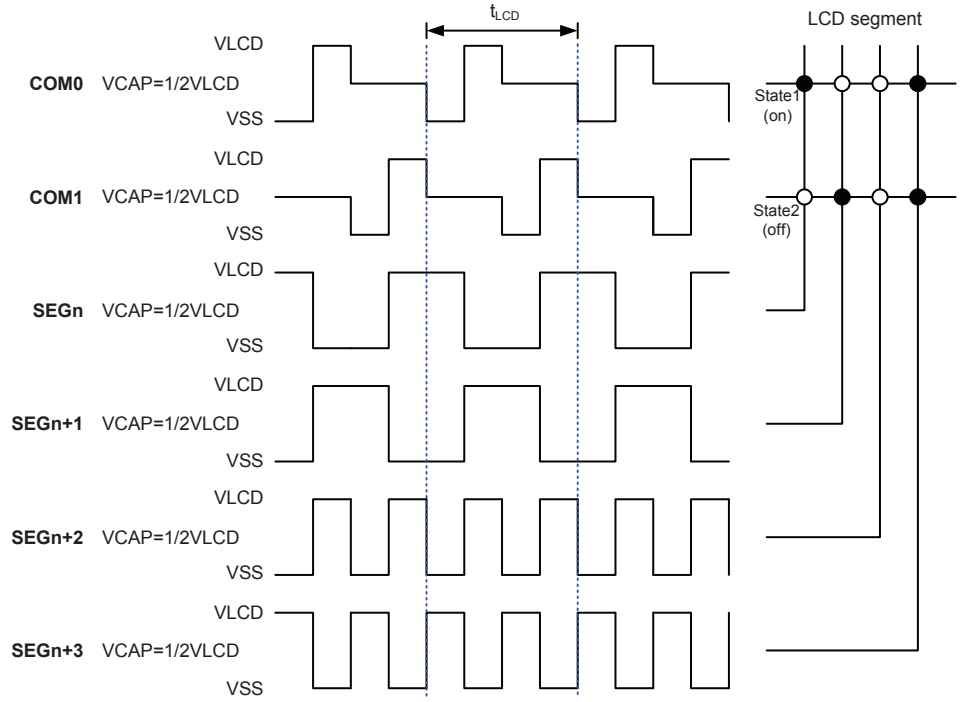
1. When the DS pin is set to '1' for 1/1 duty and 1/1 bias (static) the waveform and LCD display is as follows.



Note: $t_{LCD}=1/f_{LCD}$.

Waveforms for 1/1 Duty Drive Mode with1/1 Bias

2. When the DS pin is set to '0' for 1/2 duty and 1/2 bias, the waveform and LCD display is as follows.



Note: $t_{LCD}=1/f_{LCD}$.

Waveforms for 1/2 Duty Drive Mode with1/2 Bias

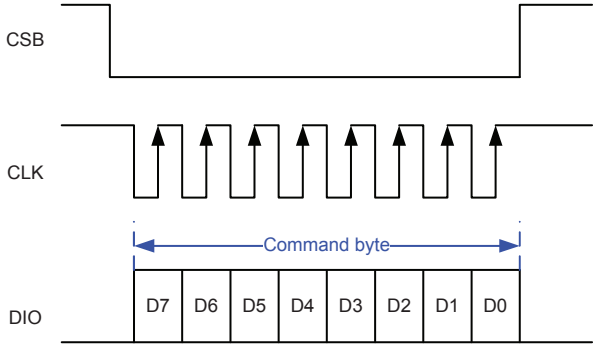
SPI 3-wire Interface

The device includes an SPI 3-wire interface.

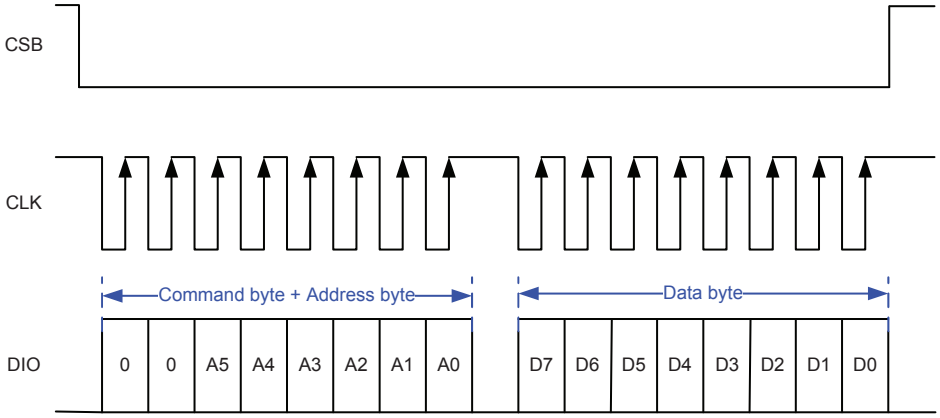
- The CSB pin is used to identify the transmitted data. The transmission is controlled by the active low signal, CSB. After the CSB falls to a low level, the data can start transmission.
- Data is transferred from the MSB of each byte (MSB First) and the data is shifted into a register on the CLK rising edge.
- The input data are automatically loaded into a register for every 8 bits of input data and the sequence starts from the CSB signal falling edge.
- For the read mode, the DIO pin is setup in the output mode after sending the read command code and setting address value.

Write Operation

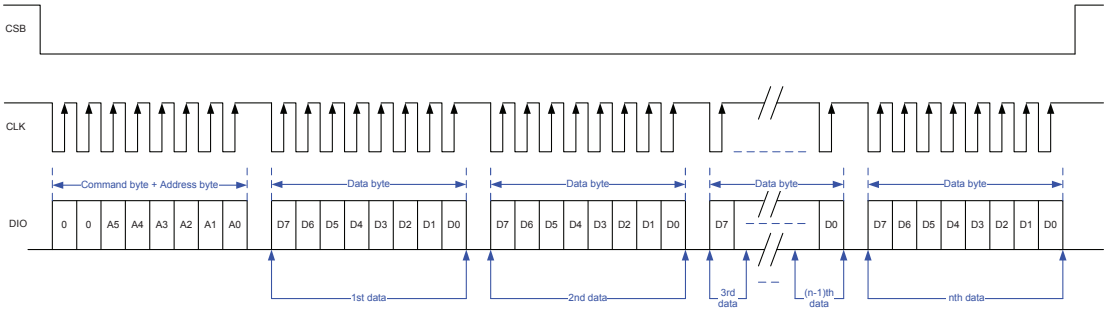
1. Write Command Byte Operation



2. Write Single Display Data Byte Operation



3. Write Pages Display Data Byte Operation



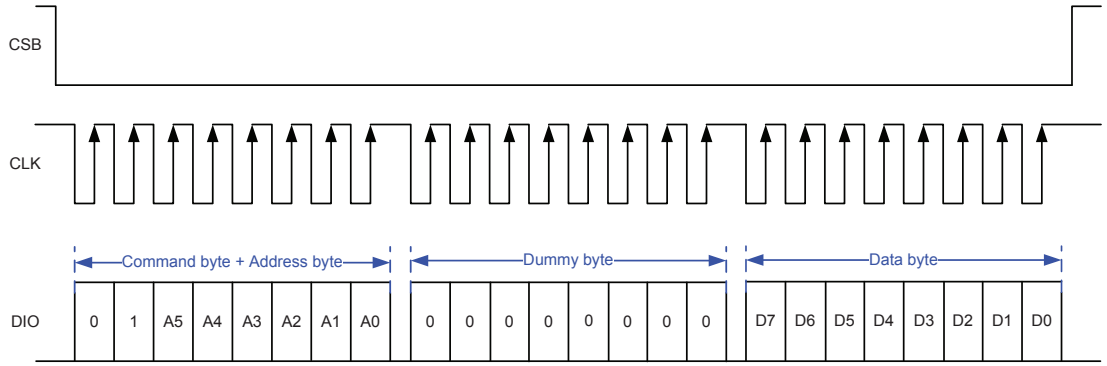
Notes that the address will continuously increment automatically and will wrap around to address 0x00H when it exceeds the maximum address.

The maximum address is shown in the following table.

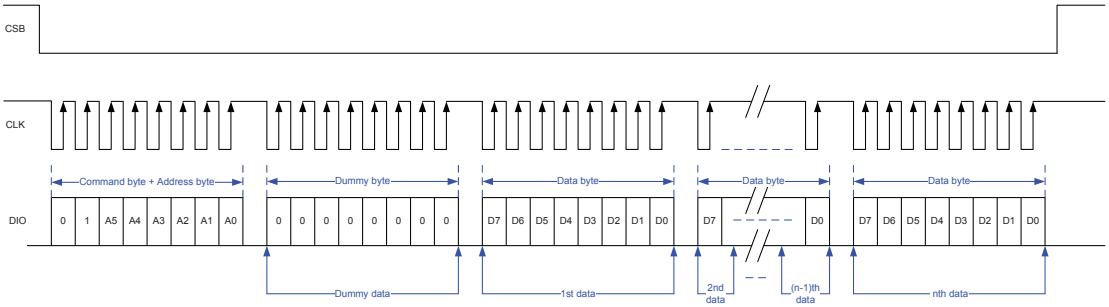
Duty	Maximum Address
1/1	1Dh
1/2	3Bh

Read Display RAM Data Operation

1. Read single display data byte operation



2. Read pages display data byte operation



Notes that the address will continuously increment automatically and will wrap around to address 0x00H when it exceeds the maximum address.

The maximum address is shown in the following table.

Duty	Maximum Address
1/1	1Dh
1/2	3Bh

Program Instruction Description

Command	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Def.	Description
RAM R/W Command											
Write Display Data	W	0	0	A5	A4	A3	A2	A1	A0	00h	Write display RAM and address set
	W	D7	D6	D5	D4	D3	D2	D1	D0	—	Display data Range: 00h~1Dh for 1COM Range: 00h~3Bh for 2COM
Read Display Data	W	0	1	A5	A4	A3	A2	A1	A0	40h	Read display RAM and address
	R	0	0	0	0	0	0	0	0	—	Dummy byte
	R	D7	D6	D5	D4	D3	D2	D1	D0	—	Display data Range: 00h~1Dh for 1COM Range: 00h~3Bh for 2COM
Function Command											
System mode	W	1	0	X	FS	F	D	S	L	80H	L: Control LCD display on/off S: Control internal system oscillator on/off D: Control LED display on/off F: Set Frame Frequency FS: OSC frequency select
LED Luminance control	W	1	1	E1	E0	P3	P2	P1	P0	C0h	E1~E0: Select LED0~LED3 output set P3~P0: 16 luminance steps controlled by PWM adjustment

Notes: 1. X: Don't care.

2. Def.: Power on reset default.

3. If the programmed command is not defined the function will not be affected.

System Mode

This command controls the system oscillator on/off, display on/off, LED on/off and Frame Frequency.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
System mode	W	1	0	X	FS	F	D	S	L	80h

FS	OSC Frequency Select	Remarks
0	51.2kHz @ 5.0V	Default
1	51.2kHz @ 3.3V	

F	Frame frequency	Remarks
0	100Hz	Default
1	200Hz	

D	LED Display	Remarks
0	off	Default
1	on	

S	OSC	Remarks
0	off	1. Default 2. Standby mode
1	on	

L	LCD Display	Remarks
0	off	Default
1	on	

LED Luminance Control

The LED port is an NMOS output structure. Data is written to the LED port using a write command, starting from the most significant bit. For such applications (see application circuits) the external LED is connected between this NMOS output structure and the VLCD pin.

- When the LEDON bit of the system mode command control register is set to 0 the LED PWM function will be disabled and the LED0~LED3 pins will be turned off.
- When the LEDON bit of the system mode command control register is set to 1 the LED PWM function will be enabled and the LED0~LED3 pins will be turned on. The LEDs will be illuminated and the luminance can be controlled with the LED PWM luminance setting command to the corresponding LED0~LED3.

Command	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Def.
LED Luminance Control	W	1	1	E1	E0	P3	P2	P1	P0	C0H

The relationship between E[0:1] and the LED luminance control for each LED pin is shown as follows.

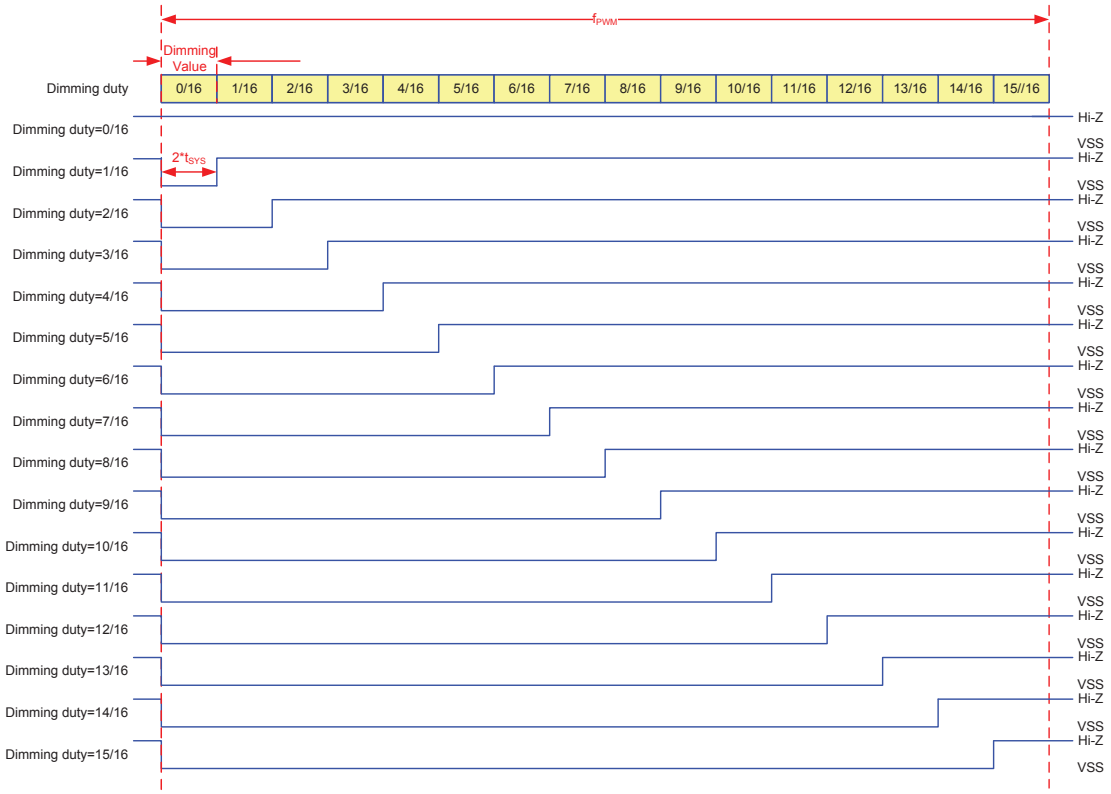
E1	E0	LED pin
0	0	LED0 – default
0	1	LED1
1	0	LED2
1	1	LED3

PWM Data Table

The relationship between the 16-step PWM value P[3:0] and the dimming duty is shown as follows.

LED PWM Luminance Setting				Dimming Duty	Note
P[3]	P[2]	P[1]	P[0]		
0	0	0	0	0/16	Lowest LED Luminance – default
0	0	0	1	1/16	
0	0	1	0	2/16	
0	0	1	1	3/16	
0	1	0	0	4/16	
0	1	0	1	5/16	
0	1	1	0	6/16	
0	1	1	1	7/16	
1	0	0	0	8/16	
1	0	0	1	9/16	
1	0	1	0	10/16	
1	0	1	1	11/16	
1	1	0	0	12/16	
1	1	0	1	13/16	
1	1	1	0	14/16	
1	1	1	1	15/16	Highest LED Luminance

The relationship between the LED waveform and dimming duty at is shown as follows.



Notes: 1. The status of the "L" bit in the system mode command control register is set to 1 and the LED luminance control command must be input data

2. The LED output status is not influenced by the display OFF command setting

3. The LED light ON/OFF function is not concerned with the segment output status

4. The LED light ON/OFF function is not controlled by the TEST pin and test function

5. Hi-Z means that LED pin is an NMOS open-drain type

6. $t_{PWM}=1/f_{PWM}=(32/51.2kHz)=625\mu s$

Write Display Data

This command can program the LCD panel display status. There is a one-to-one correspondence between the display memory addresses and the SEG outputs and between the individual bits of a RAM word and the column outputs. The following shows the RAM to LCD pattern mapping.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Write Display Data	W	0	0	A5	A4	A3	A2	A1	A0	00h
	W	D7	D6	D5	D4	D3	D2	D1	D0	—

Read Display Data

The read display RAM data format is as follows.

Command	R/W	Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Def.
Read Display Data	W	0	1	A5	A4	A3	A2	A1	A0	40h
	R	0	0	0	0	0	0	0	0	—
	R	D7	D6	D5	D4	D3	D2	D1	D0	—

Power Supply Sequence

- If the power is individually supplied on the VLCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

Holtek Power Supply Sequence Requirement:

1. Power-on sequence:

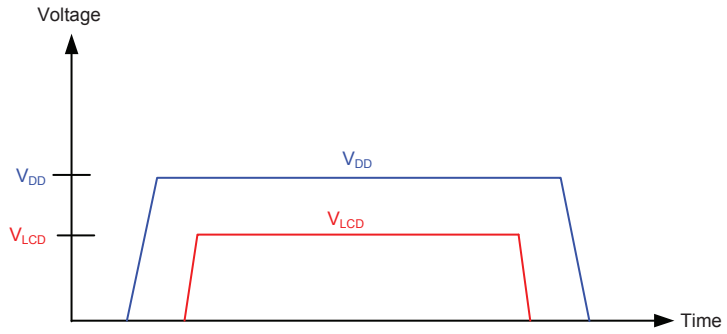
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.

2. Power-off sequence:

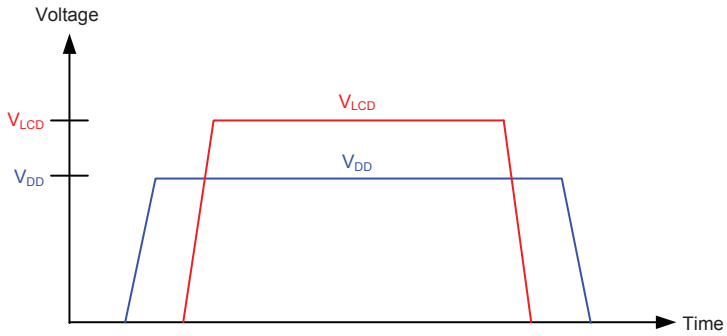
   Turn off the LCD driver power supply V_{LCD} first and then turn off the logic power supply V_{DD}.

3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

- When the V_{LCD} voltage is smaller than V_{DD} voltage application:

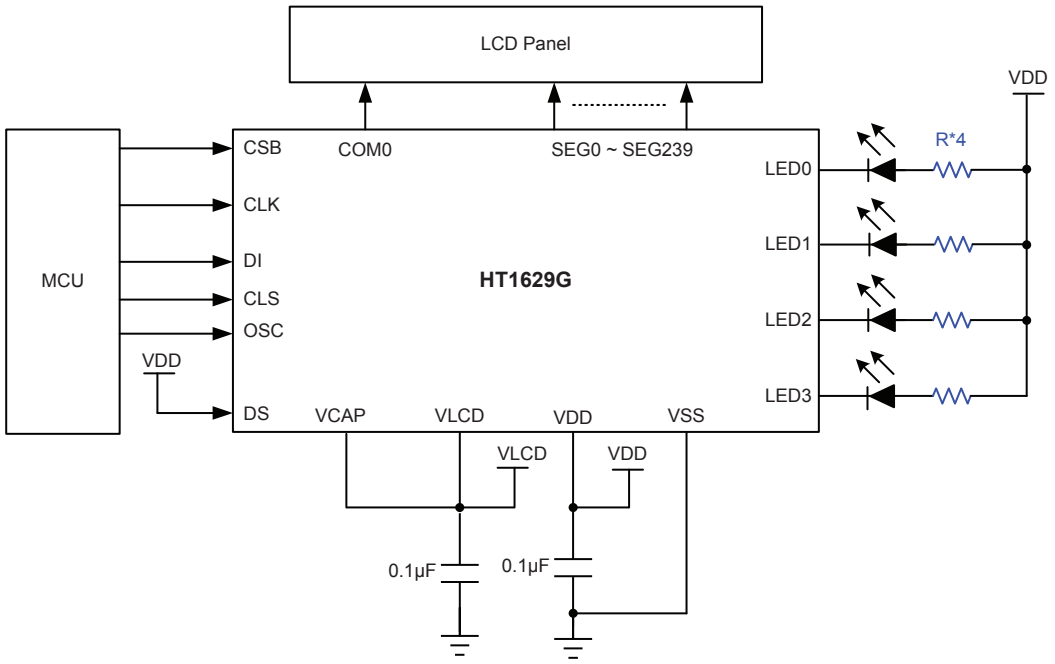


- When the V_{LCD} voltage is greater than V_{DD} voltage application:



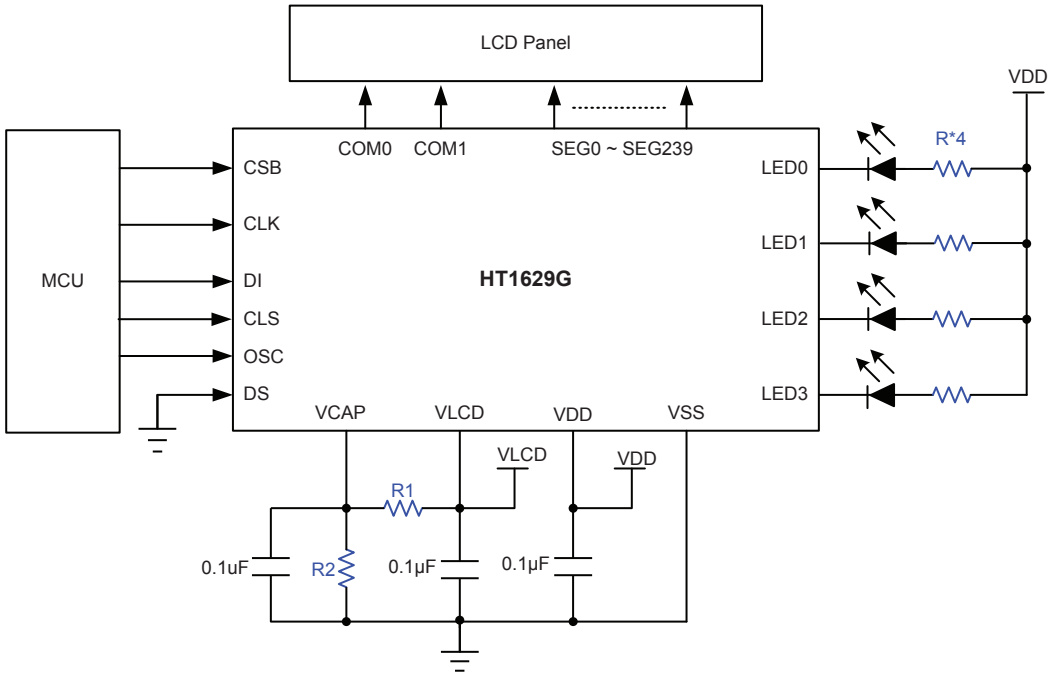
Application Circuits

DS='1', static



Note: Values of the R resistors are selected depending on the power consumption of the LEDs.

DS='0', 1/2 duty



Notes: 1. The R resistor values are selected depending upon the LED power consumption.

2. The R1 and R2 resistor values are selected depending on the LCD panel bias voltage.

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information