

AD153A Datasheet

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AD153A Features

CPU Core

- 32-bit CPU, Built-in ICACH, can be connected to Flash for expansion of code
- The main frequency is up to 120MHz

Memory

- Built-in 20Kbytes of SRAM

Clock Source

- RC Clock frequency about 16MHz
- LRC(low power RC) clock frequency about 200KHz

Digital I/O

- Up to 20 programmable digital I/O pins
- General the IO supports pull-up(10k), pull-down(60k), strong, weak output, input and high impedance
- Up to 12 external interrupt/wake-up source(low power available, can be multiplexed to any I/O, with hardware filter)
- Input channel and Output channel, provide arbitrary IO input and output options for some modules

Digital peripherals

- Two UART Controllers(UART0/1) supports DMA and Flow Control
- Two SPI Controllers with DMA(SPI0/1)

support master mode and slave mode

- Built-in Spi Flash to run code
- One SD host controller
- Three 32-bit Asynchronous Divider Timers
- One IIC Controller
- Four channel PWM output
- Infrared remote control decoder
- Watchdog

Analog Peripherals

- 0.5 watt Class-D audio amplifier output
- 10-bit high precision ADC
- Low voltage protection
- Power on reset

Operating Conditions

- Working voltage
VBAT: 2.0v - 5.5v
VDDIO: 2.0v - 3.4v
- Soft-off current is 2uA
- Operating Temperature: -40°C to +85°C

Package

- QSOP24

Application

- Universal Microcontroller
- Sound Toy
- Audio player

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1、 Pin Definition

1.1 Pin Assignment

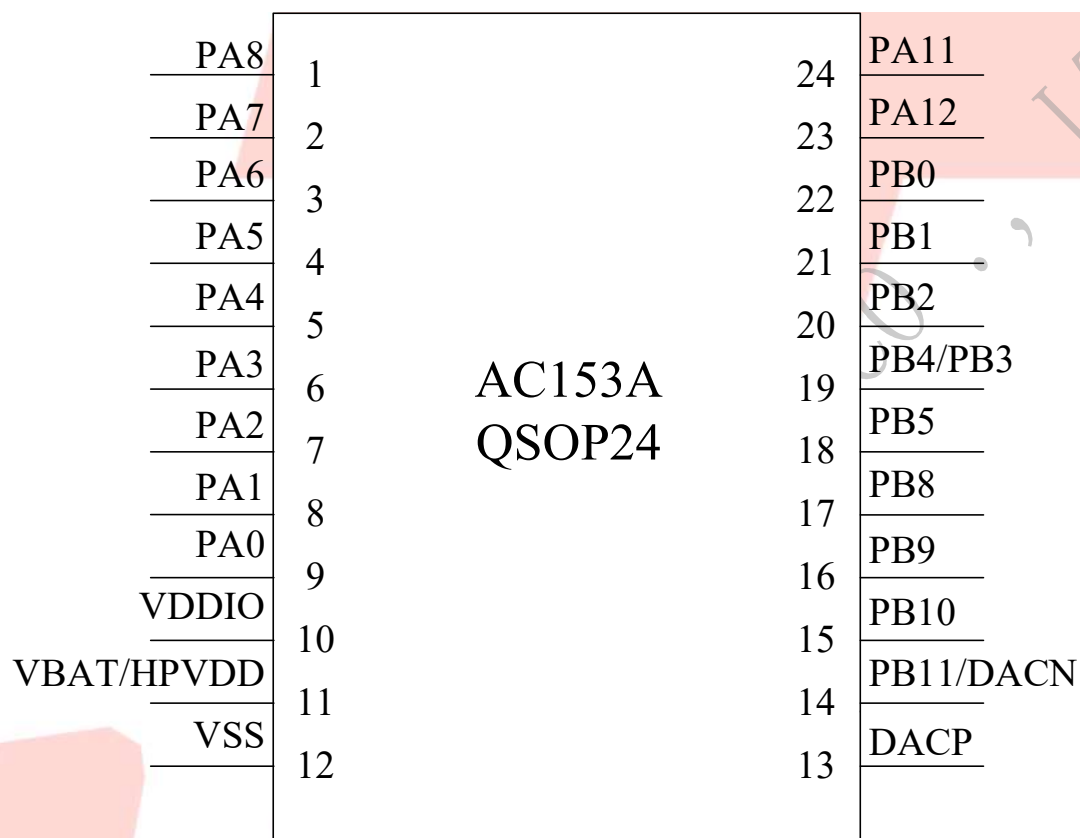


Figure 1-1 AD153A_QSOP24 Package Diagram

1.2 Pin Description

Table 1-1 AD153A_QSOP24 Pin Description

PIN NO.	Name	Type	Drive (mA)	Function	Description
1	PA8	I/O	8/64	GPIO	SPI1DIC:SPI1 Data In(C); SD0DATD:SD0 Data(D);
2	PA7	I/O	8/64	GPIO	ADC7:ADC Input Channel 7; SPI1DOC:SPI1 Data Out(C); SD0CMD:SD0 Command(D); UART0RXA:Uart0 Data In(A); I2C_SDA(C); MPWM1:PWM Channel1 Output;
3	PA6	I/O	8/64	GPIO	ADC6:ADC Input Channel 6; SPI1CLKC:SPI1 Clock(C); SD0CLKD:SD0 Clock(D); UART0TXA:Uart0 Data Out(A); I2C_SCL(C); TMR2:Timer2 Clock In; MPWM0:PWM Channel0 Output;
4	PA5	I/O	8/64	GPIO	ADC5:ADC Input Channel 5; SPI0DAT3:SPI0 Data 3 UART1RXA:Uart1 Data In(A);
5	PA4	I/O	8/64	GPIO	ADC4:ADC Input Channel 4; SPI0DAT2:SPI0 Data 2; UART1TXA:Uart1 Data Out(A); LVD:Low Voltage Detect;
6	PA3	I/O	8/64	GPIO	ADC3:ADC Input Channel 3; SPI0DIB(1):SPI0 Data1 In(B); SD0DATA:SD0 Data(A); CLKOUT; PWM2(B); MCAP0:Motor Timer0 Capture;
7	PA2	I/O	8/64	GPIO	ADC2:ADC Input Channel 2; SPI0DOB(0):SPI0 Data0 Out(B); SD0CMDA:SD0 Command(A); I2C_SDA(B); PWM2(A);

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8	PA1	I/O	8/64	GPIO	ADC1:ADC Input Channel 1; SPI0CLKB:SPI0 Clock(B); SD0CLKA:SD0 Clock(A); UART0RXB:Uart0 Data In(B); I2C_SCL(B); CAP2:Timer2 Capture;
9	PA0	I/O	8/64	GPIO (pull up)	Long Press Reset; ADC0:ADC Input Channel 0; UART0TXB:Uart0 Data Out(B);
10	VDDIO	P	/		Digital Power; (Internal linear regulator output)
11	VBAT	P	/		Battery Power Supply;
	HPVDD	P	/		Class-D APA Power Supply;
12	VSS	G	/		Ground;
13	DACP	O	/		Class-D APA Positive Output;
14	DACN	O	/		Class-D APA Negative Output;
	PB11	I/O	8	GPIO (High Voltage Resistance)	OSCIB:Crystal Oscillator Input(B);
15	PB10	I/O	8	GPIO (pull up) (High Voltage Resistance)	MCLR(0 effective);
16	PB9	I/O	8	GPIO (High Voltage Resistance)	SPI1DOD:SPI1 Data Out(D); UART1TRXB:Uart1 Data In/Out(B); I2C_SDA(D); CAP1:Timer1 Capture;
17	PB8	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKD:SPI1 Clock(D); I2C_SCL(D); OSCIA:Crystal Oscillator Input(A);
18	PB5	I/O	8/64	GPIO	ADC13:ADC Input Channel 13;
19	PB4	I/O	8/64	GPIO	ADC12:ADC Input Channel 12;
	PB3	I/O	8/64	GPIO	TDM_MCLK;
20	PB2	I/O	8/64	GPIO	SPI1DIA:SPI1 Data In(A); SD0DATB:SD0 Data(B); TDM_DAT;
21	PB1	I/O	8/64	GPIO (pull down)	ADC11:ADC Input Channel 11; SPI1DOA:SPI1 Data Out(A); SD0CMDB:SD0 Command(B); I2C_SDA(A); TDM_SYN;

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22	PB0	I/O	8/64	GPIO (pull down)	ADC10:ADC Input Channel 10; SPI1CLKA:SPI1 Clock(A); SD0CLKB:SD0 Clock(B); I2C_SCL(A); TDM_CLK;
23	PA12	I/O	8/64	GPIO	MPWM3:PWM Channel3 Output;
24	PA11	I/O	8/64	GPIO	TMR0:Timer0 Clock In; MPWM2:PWM Channel2 Output;

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2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
HPVDD	Class D Audio Power Amplifier	-0.3	5.5	V
V _{VDDIO33}	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	—
V _{HPVDD}	Voltage Input	2.0	3.7	5.5	V	—
V _{VDDIO}	Voltage output	2.0	3.0	3.4	V	VBAT = 3.7V, 100mA loading
I _{VDDIO}	Loading current	—	—	100	mA	VBAT=3.7V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	—	0.3* VDDIO	V	VDDIO = 3.3V
V _{IH}	High-Level Input Voltage	0.7* VDDIO	—	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V _{OL}	Low-Level Output Voltage	—	—	0.33	V	VDDIO = 3.3V
V _{OH}	High-Level Output Voltage	2.7	—	—	V	VDDIO = 3.3V

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2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA12 PB0~PB5	8mA	64mA	10K	60K	1、PA0 default pull up 2、PB0 & PB1 default pull down 3、internal pull-up/pull-down resistance accuracy $\pm 20\%$
PB8~PB11 (High Voltage Resistance)	8mA	–	10K	60K	

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3、 Package Information

3.1 QSOP24

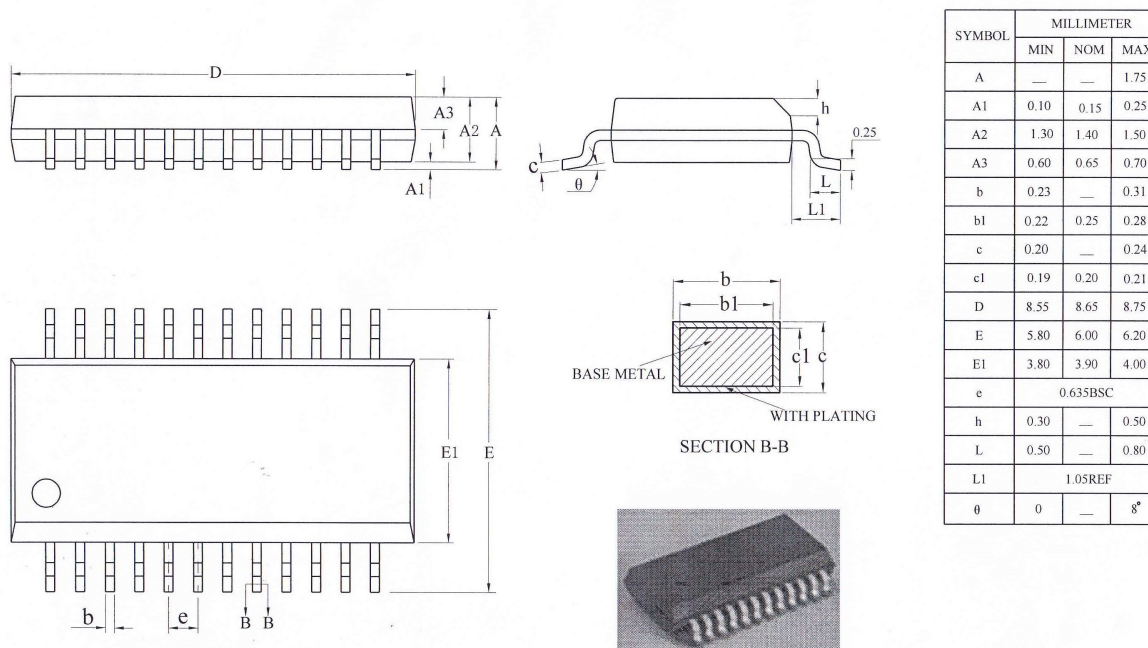
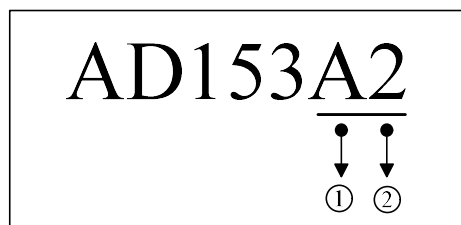


Figure 3-1. AD153A_QSOP24 Package

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4、 Package Type Specification



① Represents different packages

② Represents different memory sizes

0: No memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

5、 Revision History

Date	Revision	Description
2021.05.08	V1.0	Initial Release

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