AD156A Datasheet

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Version：V1.2

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AD156A Features

CPU Core

- 32-bit CPU,Built-in ICACH, can be connected to Flash for expansion of code
- The main frequency is up to 120MHz

Memory

- Built-in 20Kbytes of SRAM

Clock Source

- RC clock frequency about 16MHz
- LRC clock frequency about 200KHz,Accuracy ±1% at -40℃ to +85℃

Digital I/O

- Up to 28 programmable digital I/O pins
- General the IO supports pull-up(10k),pull-down(60k), strong,weak output,input and high impedance
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O, with hardware filter)
- Input channel and Output channel, provide arbitrary IO input and output options for some modules

Digital peripherals

- Two UART Controllers(UART0/1) supports DMA and Flow Control
- Two SPI Controllers with DMA(SPI0/1) support master mode and slave mode,SPI0 support 4bit,SPI1support 2bit
- Built-in Flash for code
- One SD host controller
- Three 32-bit Asynchronous Divider Timers
- One IIC Controller
- Four channel PWM output
- Infrared remote control decoder
- Watchdog

Analog Peripherals

- 0.5 watt Class-D audio amplifier output
- 14 channel 10-bit high precision ADC
- Low voltage protection
- Power on reset

Operating Conditions

- Working voltage
  VBAT: 2.0v - 5.5v
  VDDIO: 2.0v - 3.4v
- Soft-off current is 2uA
- Operating Temperature: -40°C to +85°C

Package

- QFN32(4mm*4mm)

Application

- Sound Toy
- Audio player
- Universal Microcontroller

1、Pin Definition

1.1 Pin Assignment

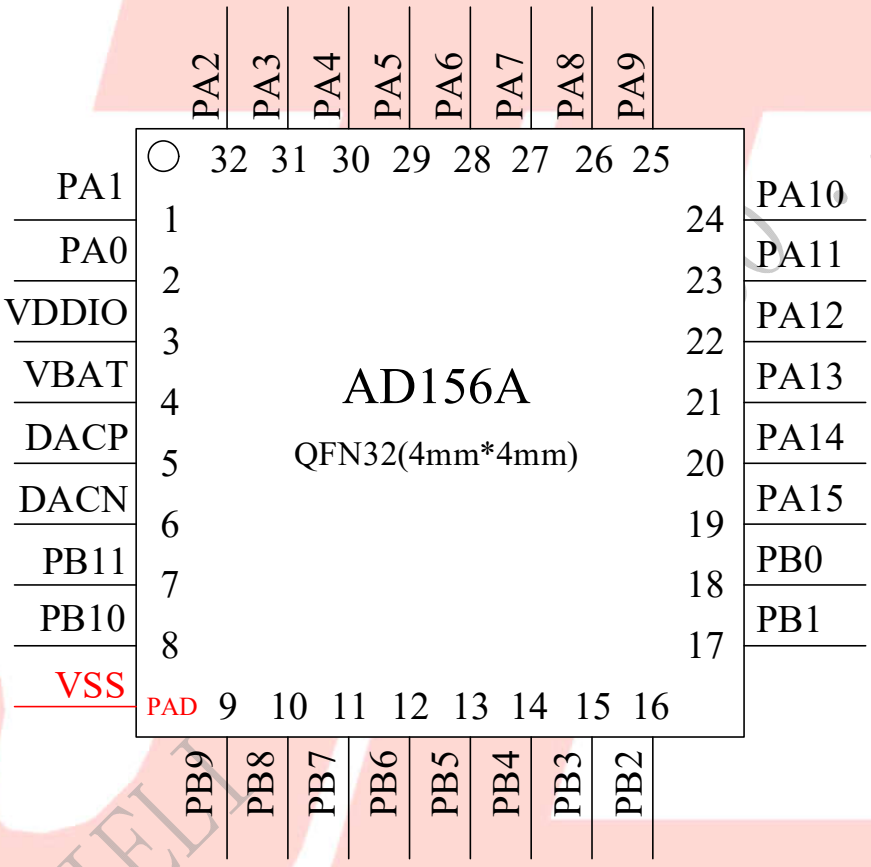


Figure 1-1 AD156A_QFN32 Package Diagram

1.2 Pin Description

Table 1-1 AD156A_QFN32 Pin Description

PIN NO.	Name	Type	Drive (mA)	Function	Description
1	PA1	I/O	8/64	GPIO	ADC1:ADC Input Channel 1; SPI0CLKB:SPI0 Clock(B); SD0CLKA:SD0 Clock(A); UART0RXB:Uart0 Data In(B); I2C_SCL(B); CAP2:Timer2 Capture;
2	PA0	I/O	8/64	GPIO (pull up)	Long Press Reset; ADC0:ADC Input Channel 0; UART0TXB:Uart0 Data Out(B);
3	VDDIO	P	/		Digital Power; (Internal linear regulator output)
4	VBAT	P	/		Battery Power Supply;
5	DACP	O	/		Class-D APA Positive Output;
6	DACN	O	/		Class-D APA Negative Output;
7	PB11	I/O	8	GPIO (High Voltage Resistance)	OSCIB:Crystal Oscillator Input(B);
8	PB10	I/O	8	GPIO (pull up) (High Voltage Resistance)	MCLR(0 effective);
9	PB9	I/O	8	GPIO (High Voltage Resistance)	SPI1DOD:SPI1 Data Out(D); UART1TRXB:Uart1 Data In/Out(B); I2C_SDA(D); CAP1:Timer1 Capture;
10	PB8	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKD:SPI1 Clock(D); I2C_SCL(D); OSCIA:Crystal Oscillator Input(A);
11	PB7	I/O	8/64	GPIO	SPI1DID:SPI1 Data In(D);
12	PB6	I/O	8/64	GPIO	SD0DATC:SD0 Data(C);
13	PB5	I/O	8/64	GPIO	ADC13:ADC Input Channel 13; SD0CMDC:SD0 Command(C);
14	PB4	I/O	8/64	GPIO	ADC12:ADC Input Channel 12; SD0CLKC:SD0 Clock(C);
15	PB3	I/O	8/64	GPIO	TDM_MCLK;

16	PB2	I/O	8/64	GPIO	SPI1DIA:SPI1 Data In(A); SD0DATB:SD0 Data(B); TDM_DAT;
17	PB1	I/O	8/64	GPIO (pull down)	ADC11:ADC Input Channel 11; SPI1DOA:SPI1 Data Out(A); SD0CMDB:SD0 Command(B); I2C_SDA(A); TDM_SYN;
18	PB0	I/O	8/64	GPIO (pull down)	ADC10:ADC Input Channel 10; SPI1CLKA:SPI1 Clock(A); SD0CLKB:SD0 Clock(B); I2C_SCL(A); TDM_CLK;
19	PA15	I/O	8/64	GPIO	ADC9:ADC Input Channel 9; SPI1DOB:SPI1 Data Out(B); MCAP3:Motor Timer3 Capture;
20	PA14	I/O	8/64	GPIO	ADC8:ADC Input Channel 8; SPI1CLKB:SPI1 Clock(B); CAP0:Timer0 Capture; MCAP2:Motor Timer2 Capture;
21	PA13	I/O	8/64	GPIO	SPI1DIB:SPI1 Data In(B); TMR1:Timer1 Clock In; MCAP1:Motor Timer1 Capture;
22	PA12	I/O	8/64	GPIO	MPWM3:PWM Channel3 Output;
23	PA11	I/O	8/64	GPIO	TMR0:Timer0 Clock In; MPWM2:PWM Channel2 Output;
24	PA10	I/O	8/64	GPIO	
25	PA9	I/O	8/64	GPIO	
26	PA8	I/O	8/64	GPIO	SPI1DIC:SPI1 Data In(C); SD0DATD:SD0 Data(D);
27	PA7	I/O	8/64	GPIO	ADC7:ADC Input Channel 7; SPI1DOC:SPI1 Data Out(C); SD0CMDD:SD0 Command(D); UART0RXA:Uart0 Data In(A); I2C_SDA(C); MPWM1:PWM Channel1 Output;

28	PA6	I/O	8/64	GPIO	ADC6:ADC Input Channel 6; SPI1CLKC:SPI1 Clock(C); SD0CLKD:SD0 Clock(D); UART0TXA:Uart0 Data Out(A); I2C_SCL(C); TMR2:Timer2 Clock In; MPWM0:PWM Channel0 Output;
29	PA5	I/O	8/64	GPIO	ADC5:ADC Input Channel 5; SPI0DAT3:SPI0 Data 3 UART1RXA:Uart1 Data In(A);
30	PA4	I/O	8/64	GPIO	ADC4:ADC Input Channel 4; SPI0DAT2:SPI0 Data 2; UART1TXA:Uart1 Data Out(A); LVD:Low Voltage Detect;
31	PA3	I/O	8/64	GPIO	ADC3:ADC Input Channel 3; SPI0DIB(1):SPI0 Data1 In(B); SD0DATA:SD0 Data(A); CLKOUT; PWM2(B); MCAP0:Motor Timer0 Capture;
32	PA2	I/O	8/64	GPIO	ADC2:ADC Input Channel 2; SPI0DOB(0):SPI0 Data0 Out(B); SD0CMDA:SD0 Command(A); I2C_SDA(B); PWM2(A);
PAD	VSS	G			Ground;

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
V_{VDDIO}	Voltage applied at VDDIO	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	VDDIO+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	_
V_{VDDIO}	Voltage output	2.0	3.0	3.4	V	VBAT = 3.7V, 100mA loading
I_{VDDIO}	Loading current	_	_	100	mA	VBAT=3.7V

2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* VDDIO	V	VDDIO = 3.0V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	_	VDDIO+0.3	V	VDDIO = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* VDDIO	V	VDDIO = 3.0V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	_	+5V	V	VDDIO = 3.0V

GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	–	–	0.1* VDDIO	V	VDDIO = 3.0V
V_{OH}	High-Level Output Voltage	0.9* VDDIO	–	–	V	VDDIO = 3.0V

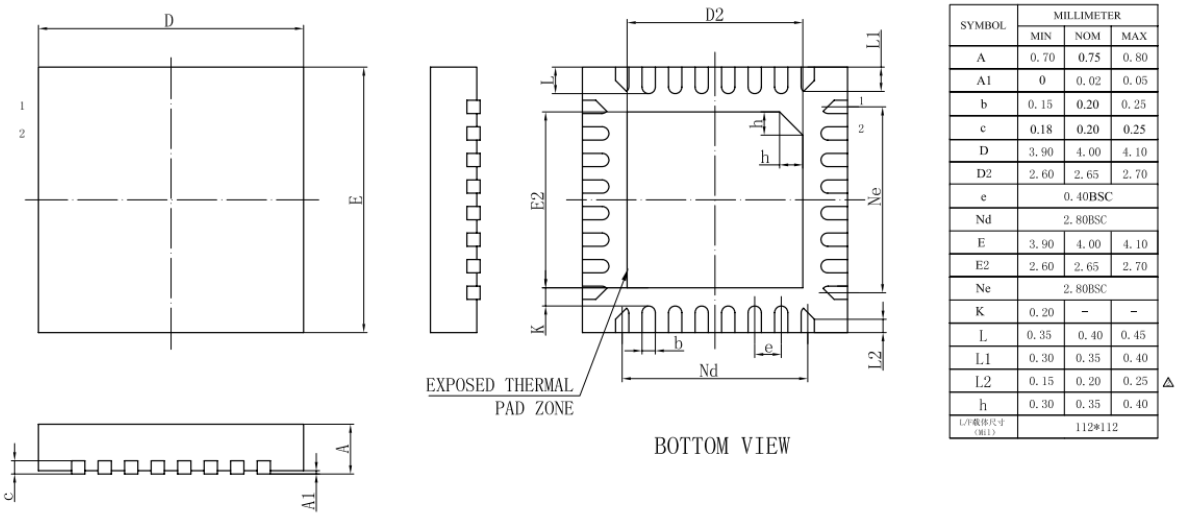
2.4 Internal Resistor Characteristics

Table 2-4

Port	**General Output**	**High Drive**	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA0~PA15 PB0~PB7	8mA	64mA	10K	60K	1、PA0&PB10 default pull up 2、PB0 & PB1 default pull down 3、internal pull-up/pull-down resistance | accuracy ±20%
PB8~PB11	8mA	–	10K	60K	

3、 Package Information

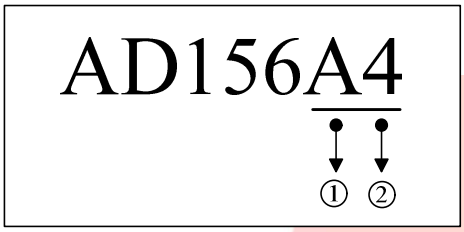
3.1 QFN32



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	–	–
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	112*112		

Figure 3-1. AD156A_QFN32 Package

4、 Package Type Specification



①Represents different packages

②Represents different memory sizes

0: No memory

2: 2Mbit Flash

4: 4Mbit Flash

8: 8Mbit Flash

5、 Revision History

Date	Revision	Description
2021.03.03	V1.0	Initial Release
2021.05.08	V1.1	parameter modification
2021.04.27	V1.2	LRC precision description