JL7018F Datasheet

Zhuhai Jieli Technology Co.,LTD

Version：1.1

Date：2022.06.08

JL7018F Features

CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash

Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects

Audio Codec

- Two channels 24-bit DAC,SNR ≥ 104dB
- Four channels 24-bit ADC,SNR ≥ 95dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/64kHz/88.2kHz/96kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Four channels analog audio inputs
- Audio DAC supports differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

ANC

- ANC processing engine up to 750 kHz sample rate
- 7.5μs analog to analog latency
- Supports 4 differential or single-ended analog inputs, 4 digital microphone inputs for ANC
- Supports 2 channels Feed-Forward, Feed-Back, Hybrid ANC
- ANC module include 20 double precision Biquad filters for each FF/FB/ music compensation control

Bluetooth

- Compliant with Bluetooth V5.3+BR+EDR+BLE specification
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with minimum -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\att\gap\gatt\rfcomm\sdp\l2cap profile
- bap 1.0\pacs 1.0\ccp 1.0\mcp 1.0\micp 1.0\vcp 1.0\csip 1.0
- a2dp 1.3.2\avctp 1.4\avdtp 1.3\ avrcp 1.6.2\hfp 1.8 \spp 1.2\rfcomm 1.1\pnp 1.3\hid 1.1.1\sdp core5.3\l2cap core 5.3

Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD
- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- I2C Master/Slave interface
- SPI Master/Slave interface
- I2S Master/Slave interface
- QDEC
- Low power CapSense
- 12-channel 10-bit ADC for analog sampling
- 4-channel Motor PWM controller
- 24 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- Less than 2uA sleep current
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V

Packages

- QFN40(5mm*5mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth Stereo Headsets and Headphones
- Bluetooth Stereo ANC Headsets and Headphones
- Bluetooth TWS ANC Earphones

1 Block Diagram

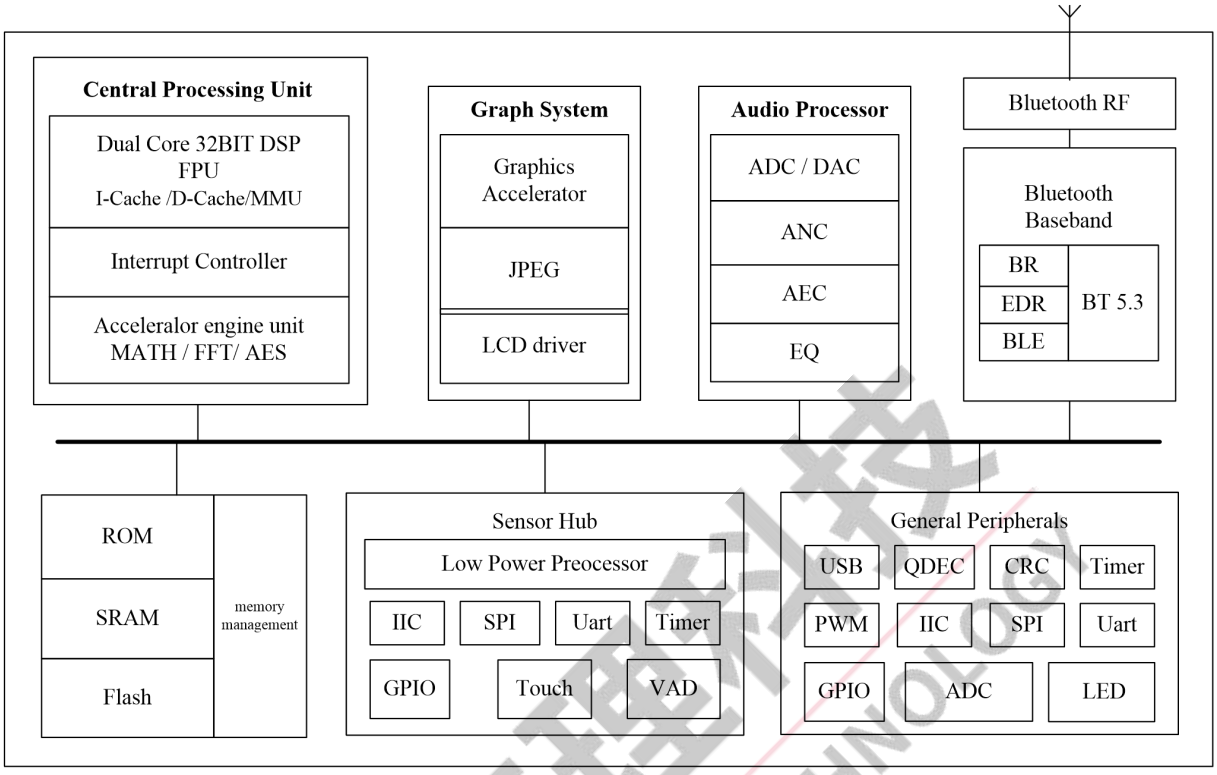


Figure 1-1 JL7018F Block Diagram

2 Pin Definition

2.1 Pin Assignment

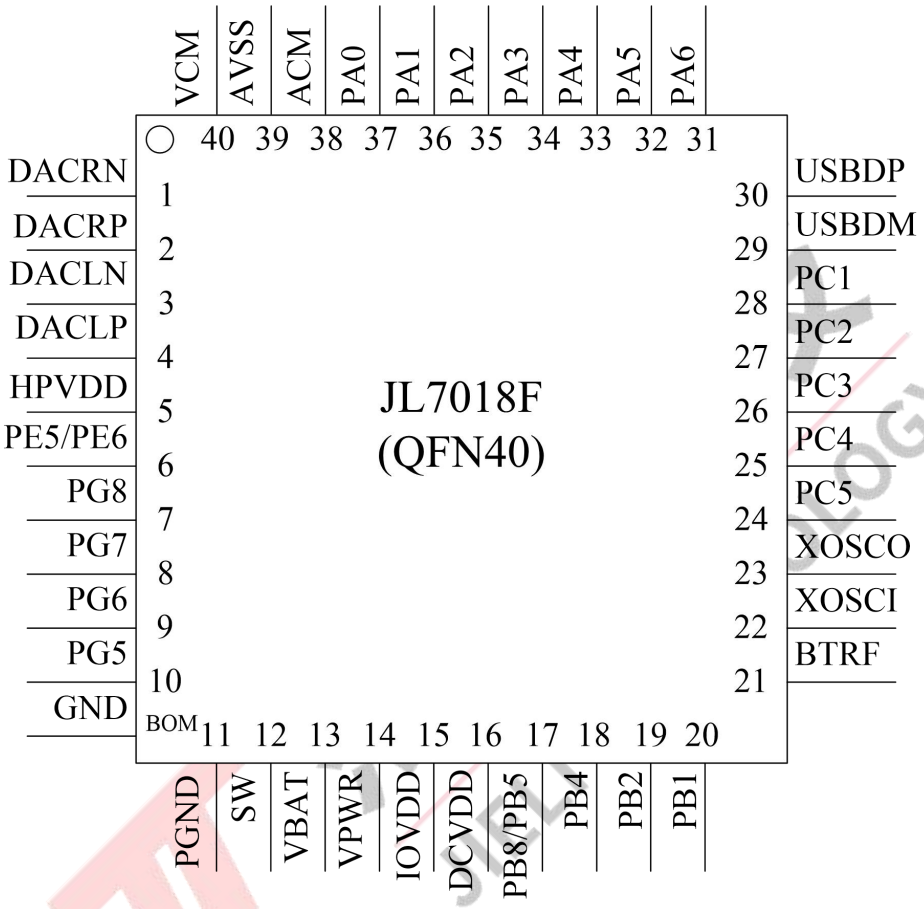


Figure 2-1 JL7018F Package Diagram

2.2 Pin Description

Table 2-1 JL7018F Pin Description

PIN NO.	Name	Type	Function	Other Function
1	DACRN	AO		Different DAC Right Negative Channel
2	DACRP	AO		Different DAC Right Positive Channel
3	DACLN	AO		Different DAC Left Negative Channel
4	DACLP	AO		Different DAC Left Positive Channel
5	HPVDD	PI		Audio power
6	PE6	I/O	GPIO	SDPG: supply voltage to SD Card
	PE5	I/O	GPIO	SPI4_D3(PSRAM): SPI4 Data3; SPI0_DAT3D: SPI0 Data3(D);
7	PG8	I/O	GPIO	MICIN2: MIC2 Input Channel 2; MIC2_P: Different MIC2 Positive; AMUX_C0:Analog Channel C0 input;
8	PG7	I/O	GPIO	MIC_BIAS2: MIC2 Bias Output(Built-in resistor); MIC2_N: Different MIC2 Negative; AMUX_C1: Analog Channel C1 input; ADC15: ADC Input Channel 15;
9	PG6	I/O	GPIO	MICIN3: MIC3 Input Channel3; MIC3_P: Different MIC3 Positive; AMUX_D0: Analog Channel D0 input; FPIN2: Fault Detect In2;
10	PG5	I/O	GPIO	MIC_BIAS3: MIC3 Bias Output(Built-in resistor); MIC3_N: Different MIC3 Negative; AMUX_D1:Analog Channel D1 input; ADC14: ADC Input Channel 14; TMR3CK: PWM Timer3 CLK In;
11	PGND	G		The ground of Buck DC-DC converter;
12	SW	PO		Switch signal of the Buck converter,connected to Inductor;
13	VBAT	P		Power Supply, connect to battery;
14	VPWR (PP0)	PI (I/O)	GPIO (High Voltage Input)	Charging Power Input; UART0TXB: Uart0 Data Out(B); UART0RXB: Uart0 Data In(B); PWM3: Timer3 PWM Output; CAP1: Timer1 Capture;
15	IOVDD	PO		Built-in linear voltage regulator output;
16	DCVDD	P		Internal Power;

17	PB8	I/O	GPIO (High Voltage Input)	EVDD: Supply voltage 1.1V; CAP4: Timer4 Capture;
	PB5	I/O	GPIO (High Voltage Input)	LP_Touch4: Low Power Touch Channel 4; IIC1_SDA_A: IIC1 SDA(A); ADC8: ADC Input Channel 8; UART3RXB: Uart3 Data In(B);
18	PB4	I/O	GPIO (High Voltage Input)	LP_Touch3: Low Power Touch Channel 3; CLKOUT0: CLK Output Channel 0; SPI4DIA: SPI4 Data In(A); IIC1_SCL_A: IIC1 SCL(A); UART3TXB: Uart3 Data Out(B); TMR2: Timer2 Clock Input;
19	PB2	I/O	GPIO (High Voltage Input)	LP_Touch2: Low Power Touch Channel 2; SPI4CLKA: SPI4 Clock(A); Q-decoder0_0: Quadrature decoder0_0; ADC7: ADC Input Channel 7; UART3TXA: Uart3 Data Out(A); CAP5: Timer5 Capture;
20	PB1	I/O	GPIO (High Voltage Input)	Hold down 0 to reset; LP_Touch1: Low Power Touch Channel 1; ADC6: ADC Input Channel 6;
21	BTRF	RFI		Bluetooth RF antenna interface;
22	XOSCI	I		System Crystal Oscillator Input;
23	XOSCO	O		System Crystal Oscillator Output;
24	PC5	I/O	GPIO	SPI0_DAT2C: SPI0 Data2(C); SD0_CLKA: SD0 Clock(A); SPI1DOB: SPI1 Data Out(B); IIC0_SDA_B: IIC0 SDA(B); ALNK_DAT3(B): Audio Link Data3(B); ADC5: ADC Input Channel 5; UART2RXA: Uart2 Data In(A);
25	PC4	I/O	GPIO	SPI0_DIC: SPI0 Data In(C); SD0CMDA: SD0 CMD(A); SPI1CLKB: SPI1 Clock(B); IIC0_SCL_B: IIC0 SCL(B); ALNK_DAT2B: Audio Link Data2(B); ADC4: ADC Input Channel 4; UART2TXA: Uart2 Data Out(A); PWM4: Timer4 PWM Output;

26	PC3	I/O	GPIO	SPI0_CSC: SPI0 Chip Select(C); SD0DATOA: SD0 Data Out(A); SPI1DIB: SPI1 Data In(B); ALNK_LRCKB: Audio Link Word Select(B); TMR3: Timer3 Clock Input;
27	PC2	I/O	GPIO	SPI0_DOC: SPI0 Data Out(C); ALNK_SCLKB: Audio Link Serial Clock(B); TMR1: Timer1 Clock Input;
28	PC1	I/O	GPIO	SPI0_CLKC: SPI0 Clock(C); ALNK_DAT1B: Audio Link Data1(B); TMR5: Timer5 Clock Input; PWMCH1L: PWM CH1 Low;
29	USBDM	I/O	USB Negative Data (pull down)	SDTAP_DATB: SDTAP Data(B); SPI2DOB: SPI2 Data Out(B); IIC0_SDA_A: IIC0 SDA(A); ADC11: ADC Input Channel 11; UART1RXB: Uart1 Data In(B);
30	USBDP	I/O	USB Positive Data (pull down)	SDTAP_CLKB: SDTAP CLK(B); SPI2CLKB: SPI2 Clock(B); IIC0_SCL_A: IIC0 SCL(A); ADC10: ADC Input Channel 10; UART1TXB: Uart1 Data Out(B);
31	PA6	I/O	GPIO	PLNK_DAT0: PLNK Data 0; SPI2DOA: SPI2 Data Out(A); ALNK_DAT3A: Audio Link Data3(A); ADC2: ADC Input Channel 2; UART0RXA: Uart0 Data In(A); CAP0: Timer0 Capture;
32	PA5	I/O	GPIO	PLNK_SCLK: PLNK Serial Clock; SPI2CLKA: SPI2 Clock(A); ALNK_DAT2A: Audio Link Data2(A); ADC1: ADC Input Channel 1; UART0TXA: Uart0 Data Out(A);
33	PA4	I/O	GPIO	MIC_BIAS1: MIC1 Bias Output(Built-in resistor); MIC1_N: Different MIC1 Negative; AMUX_B1:Analog Channel B1 input; SPI2DIA: SPI2 Data In(A); ALNK_DAT1A: Audio Link Data1(A); CAP2: Timer2 Capture;

34	PA3	I/O	GPIO	MICIN1: MIC1 Input Channel 1; MIC1_P: Different MIC1 Positive; AMUX_B0:Analog Channel B0 input; SPI1DOA: SPI1 Data Out(A); ALNK_DAT0(A): Audio Link Data0(A); PWM1: Timer1 PWM Output;
35	PA2	I/O	GPIO	MIC_BIAS0: MIC0 Bias Output(Built-in resistor); MIC0_N: Different MIC0 Negative; AMUX_A1:Analog Channel A1 input; CLKOUT1: Clock Out1; SPI1CLKA: SPI1 Clock(A); ALNK_MCLKA: ALNK Master Clock(A); UART1RXA: Uart1 Data In(A); CAP3: Timer3 Capture;
36	PA1	I/O	GPIO	MICIN0: MIC0 Input Channel 0; MIC0_P: Different MIC0 Positive; AMUX_A0:Analog Channel A0 input; SPI1DIA: SPI1 Data In(A); UART1TXA: Uart1 Data Out(A); PWM0: Timer0 PWM Output;
37	PA0	I/O	GPIO	MICLDO: MIC Power Supply; ADC0: ADC Input Channel 0;
38	ACM	P		Audio analog reference bias;
39	AVSS	P		Audio analog ground;
40	VCM	G		Audio ADC/DAC reference;
PAD	VSS	G		System Ground;

Pin Type	**Description**	**Pin Type**	**Description**
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V
V_{HPVDD}	Voltage applied at HPVDD	-0.3	+3	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.4	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	_	3.0	_	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	200	mA	IOVDD=3.2V@VBAT = 3.5V
DCVDD	Voltage output	_	1.25	_	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	100	mA	DCVDD=1.25V@IOVDD=3.0v on LDO mode
		_	_	180	mA	DCVDD=1.25V@VBAT=3.0v on DCDC mode
EVDD	Voltage output	_	1.1	_	V	DCVDD=1.25V, 1mA loading
	Loading current	_	_	5	mA	EVDD=1.1V@DCVDD=1.25v
Low Power mode						
IOVDD	Loading current	_	_	10	mA	IOVDD=3V@VBAT = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VPWR	Charge Input Voltage	4.5	5	5.5	V	_
$V_{bat\ float}$	Charge Voltage	4.15	4.2	4.25	V	VPWR＞4.5V
		4.30	4.35	4.40	V	VPWR＞4.65V
I_{bat}	Charge Current	15	_	200	mA	Charge current at fast charge mode VBAT=4.0V@VPWR=5.0V
I_{end}	End Of Charge Current	2	_	30	mA	End of charge current
V_{Trikl}	Trickle Charge Voltage	_	3.0	_	V	VPWR＞4.5V
I_{Trikl}	Trickle Charge Current	1.5	_	30	mA	V_{BAT}<V_{Trikl}

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	_	_	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Output Voltage	0.9* IOVDD	_	_	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive(mA)		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA6 PC1~PC5 PG5~PG8 PE5 , PE6	HD,HD0==0,0	2.4	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull Down 3、internal pull-up / pull-down resistance | accuracy ±20%
	HD,HD0==0,1	8			
	HD,HD0==1,0	26			
	HD,HD0==1,1	46			
PP0	8		10K	10K	
PB1~PB8	8		10K	10K	
USBDP	4		1.5K	15K	
USBDM			180K	15K	

3.6 DAC Characteristics

Table 3-6

Parameter	Min	Typ	Max	Unit	Audio Format	Test Conditions
Frequency Response	20	_	20k	Hz	_	Differential Mode 1KHz/0dB 32 ohm loading With A-Weighted Filter
Output Swing	_	1	_	Vrms	_	
THD+N	_	-77	_	dB	PCM	
	_	-70	_	dB	SBC	
S/N	_	105	_	dB	PCM	
	_	105	_	dB	SBC	
Crosstalk	_	-110	_	dB	_	1KHZ/0dB 10k ohm loading
Dynamic Range	_	104	_	dB	PCM	Differential Mode 1KHz/-60dB 32 ohm loading With A-Weighted Filter
	_	104	_	dB	SBC	
Noise Floor	_	5.6	_	uVrms	_	A-Weighted Filter
DAC Output Power	_	32	_	mW	_	Differential Mode 32ohm loading

3.7 ADC Characteristics

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		94		dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
SNR	_	95	_	dB	Fsample=44.1kHz,Gain=0dB
THD+N	_	-75	_	dB	Fin=1KHz 590mVrms
SNR	_	76	_	dB	Fsample=44.1kHz,Gain=18dB
THD+N	_	-73	_	dB	Fin=1KHz 75mVrms

3.8 BT Characteristics

3.8.1 Transmitter

Basic Data Rate Table 3-8

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			7.0	9	dBm	25℃, Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Power Control Range			18.2		dB	
20dB Bandwidth			950		KHz	
Adjacent Channel Transmit Power	+2MHz		-28		dBm	
	-2MHz		-34		dBm	
	+3MHz		-30		dBm	
	-3MHz		-43		dBm	

Enhanced Data Rate Table 3-9

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1.9		dB	25℃, Power Supply VBAT=3.7V 2441MHz 4 Layer Board
π/4 DQPSK Modulation Accuracy	DEVM RMS		5.14		%	
	DEVM 99%		9.03		%	
	DEVM Peak		14.22		%	
Adjacent Channel Transmit Power	+2MHz		-28		dBm	
	-2MHz		-34		dBm	
	+3MHz		-30		dBm	
	-3MHz		-43		dBm	

3.8.2 Receiver

Basic Data Rate **Table 3-10**

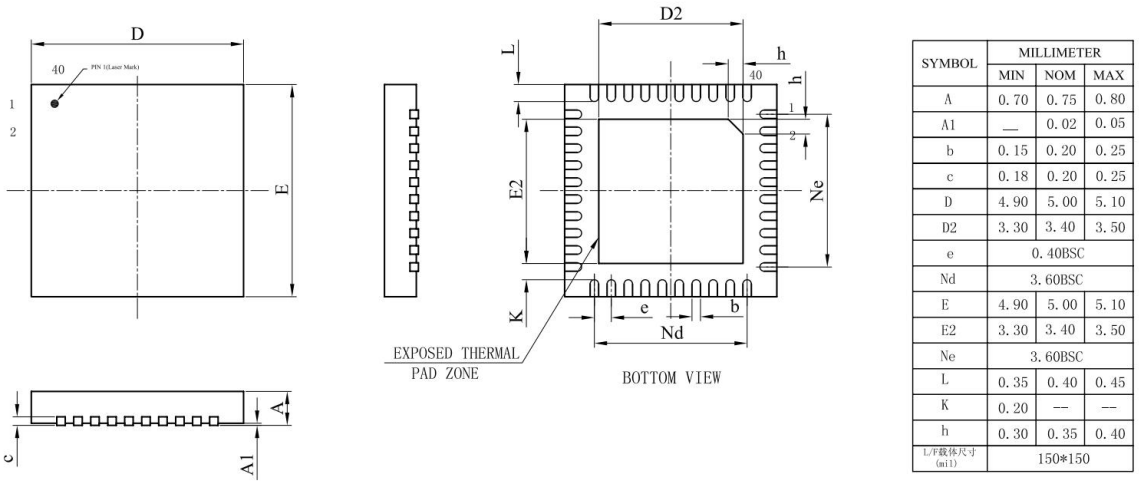
Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25℃, Power Supply VBAT=3.7V 2441MHz DH5 4 Layer Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-29		dB	
	+3MHz		-45		dB	
	-3MHz		-23		dB	

Enhanced Data Rate **Table 3-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-95	-94		dBm	25℃, Power Supply VBAT=3.7V 2441MHz 2DH5 4 Layer Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel Interference Rejection	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-29		dB	
	+3MHz		-45		dB	
	-3MHz		-23		dB	

4 Package Information

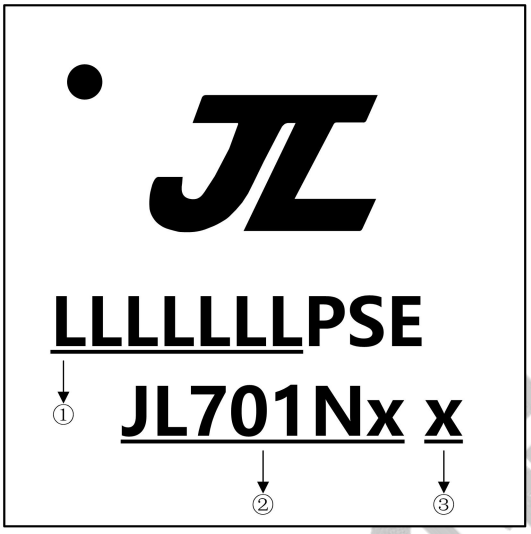
4.1 QFN40_5.0x5.0



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	150*150		

Figure 4-1 JL7018F Package

5 IC Marking Information



① LLLLLLL：Production Batch
② JL701Nx：Chip Model
③ x：Built-in flash size
0: No Flash Memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash

6 Solder-Reflow Condition

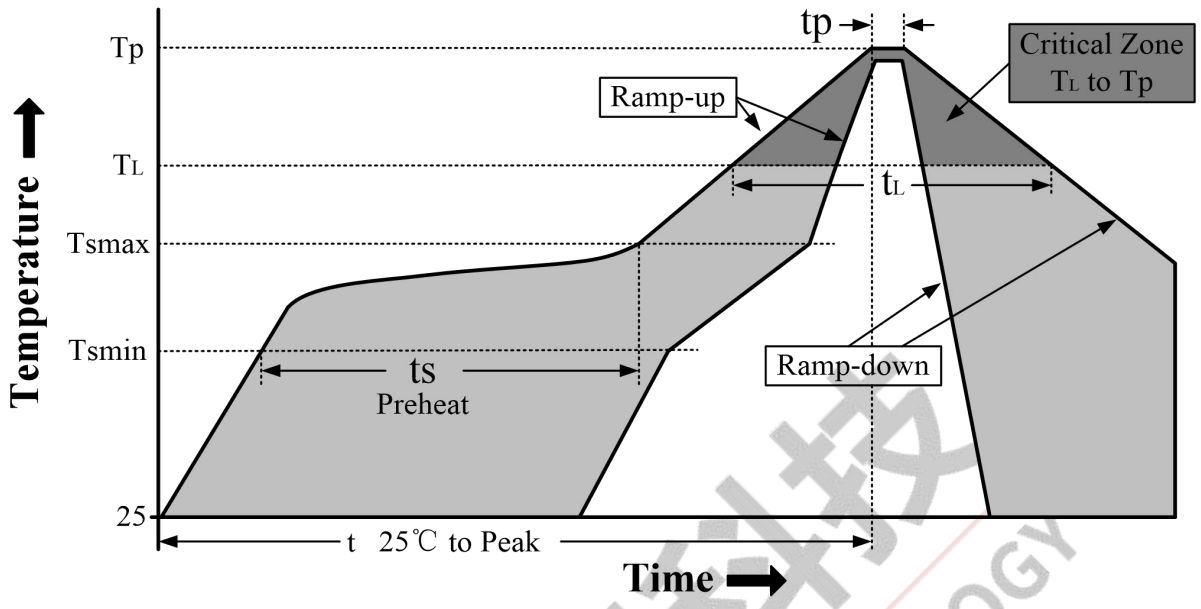


Figure 6-1 Classification Reflow Profile

Classification Profiles **Table 6-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100℃	150℃
	Temperature Max (T_{smax})	150℃	200℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183℃ 60-150 seconds	217℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5℃ of actual Peak Temperature (tp)[2]		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6℃/second max	6℃/second max
Time 25℃ to peak temperature		6 minutes max	8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a "supplier" minimum and "user" maximum.

SnPb - Classification Temperature **Table 6-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ⩾ 350
<2.5 mm	240 +0/-5℃	225 +0/-5℃
⩾2.5 mm	225 +0/-5℃	225 +0/-5℃

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260℃	260℃	260℃
1.6 mm - 2.5mm	260℃	250℃	245℃
> 2.5mm	250℃	245℃	245℃

7 Revision History

Date	Revision	Description
2022.04.09	V1.0	Initial Release
2022.06.08	V1.1	Add Block Diagram &IC Marking Information & Solder-Reflow Condition